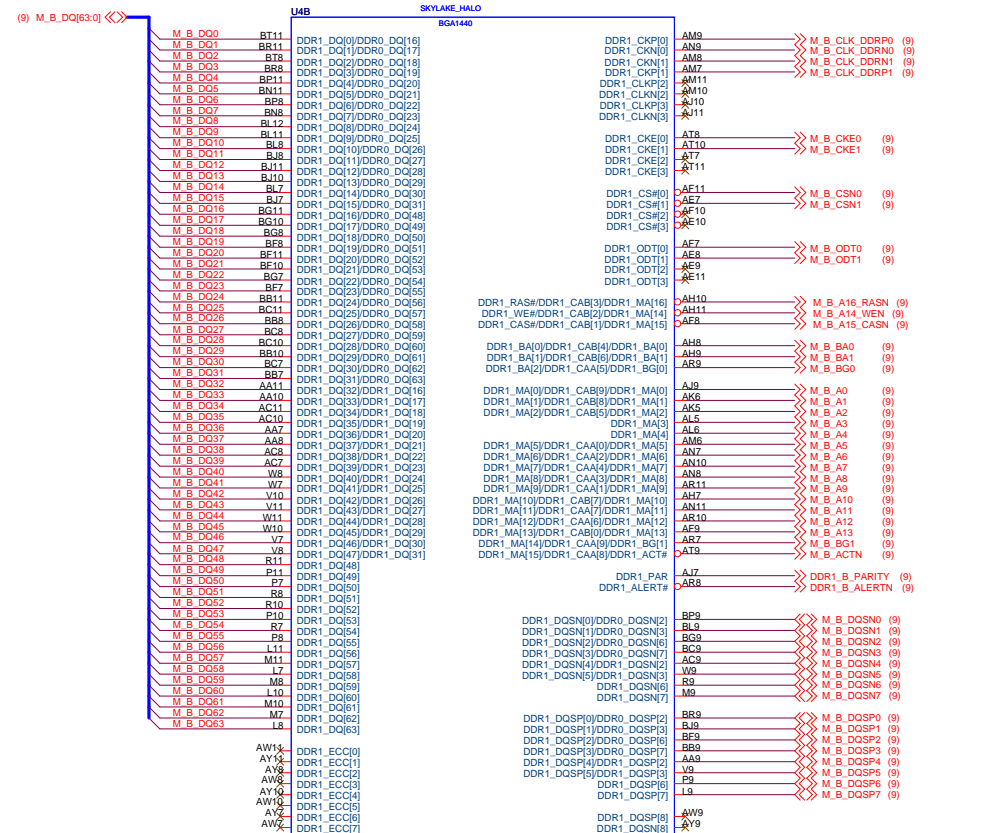
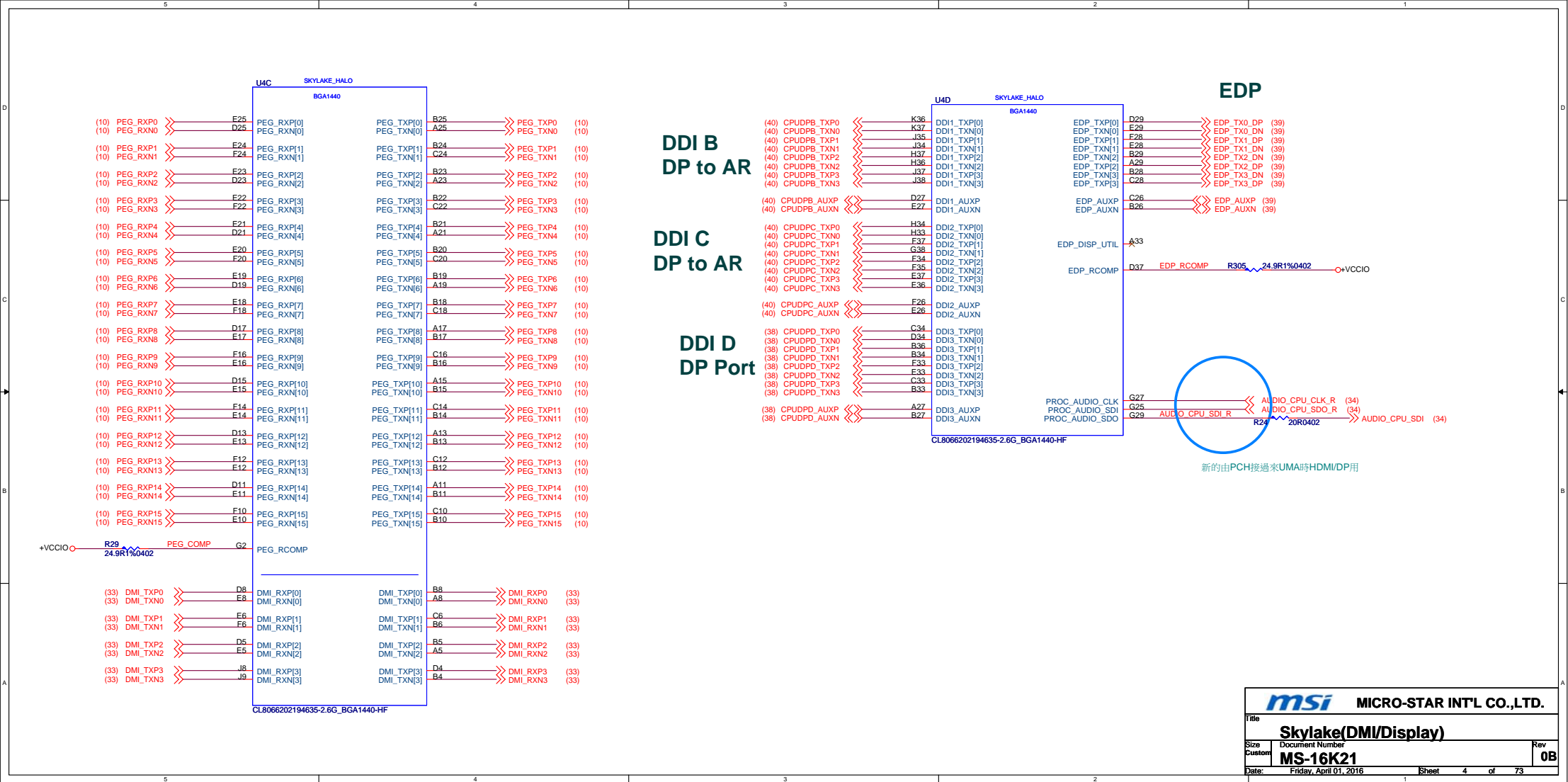
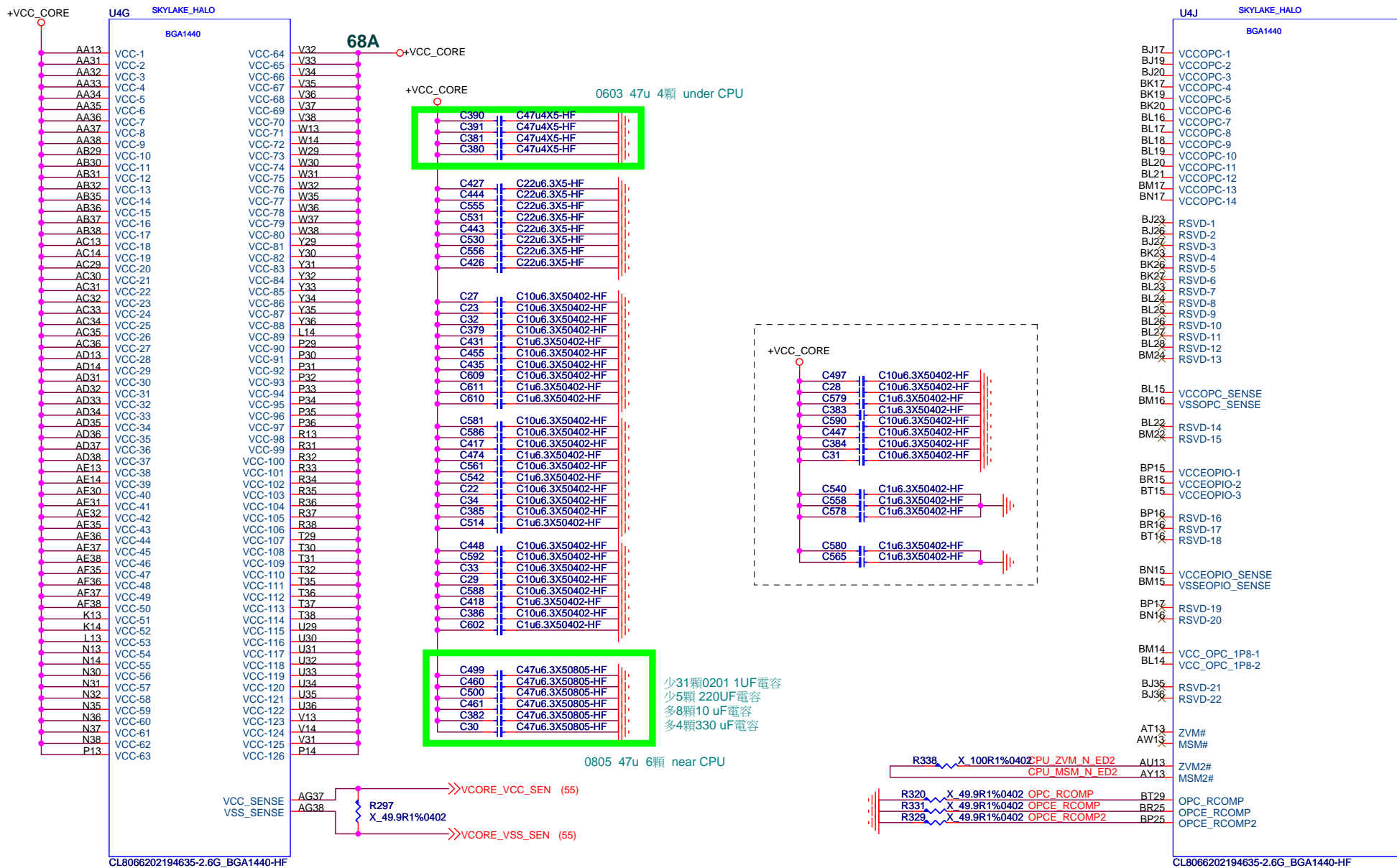


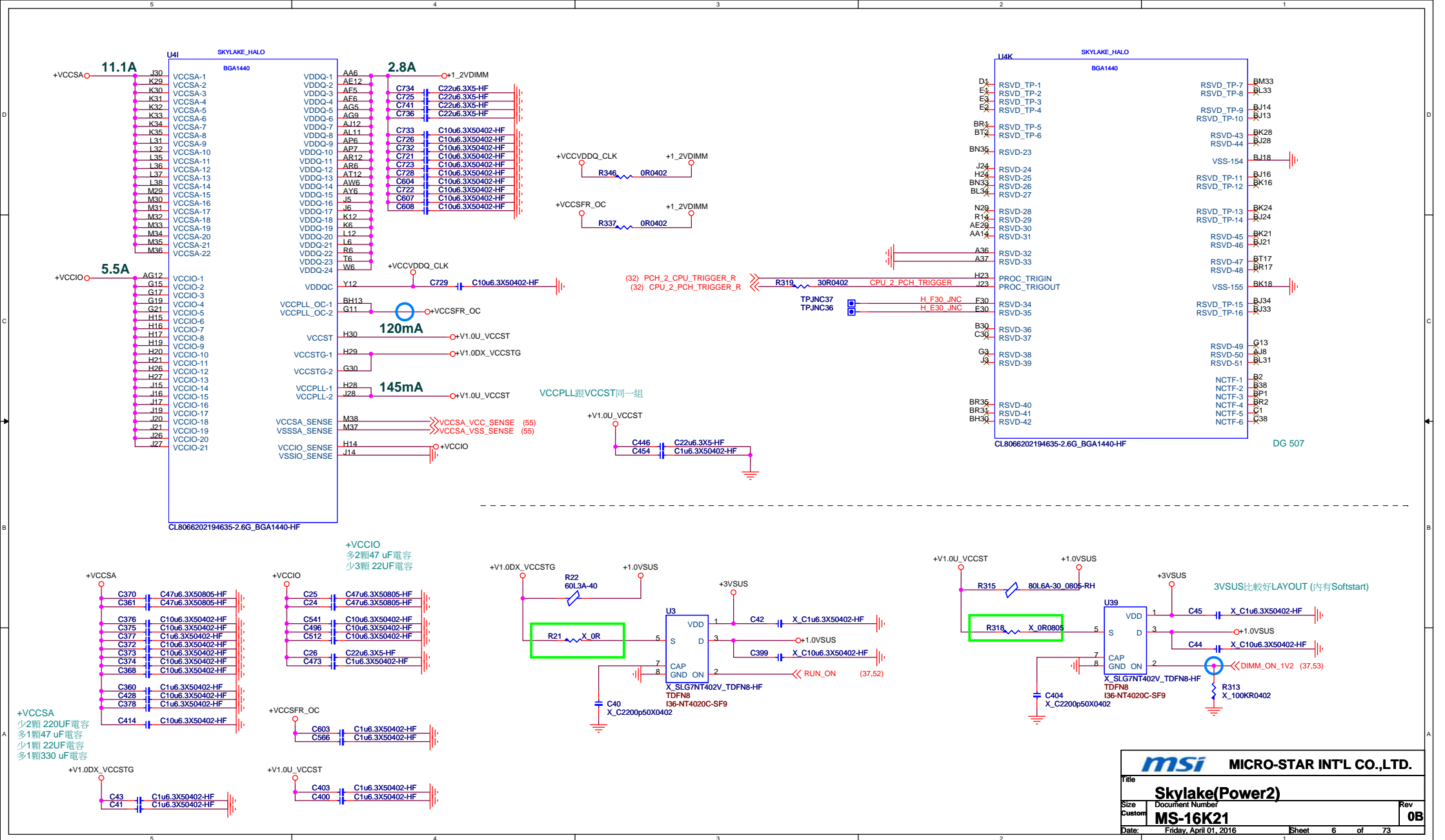
DDR Channel B

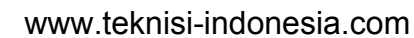


CL8066202194635-2.6G_BGA1440-HF

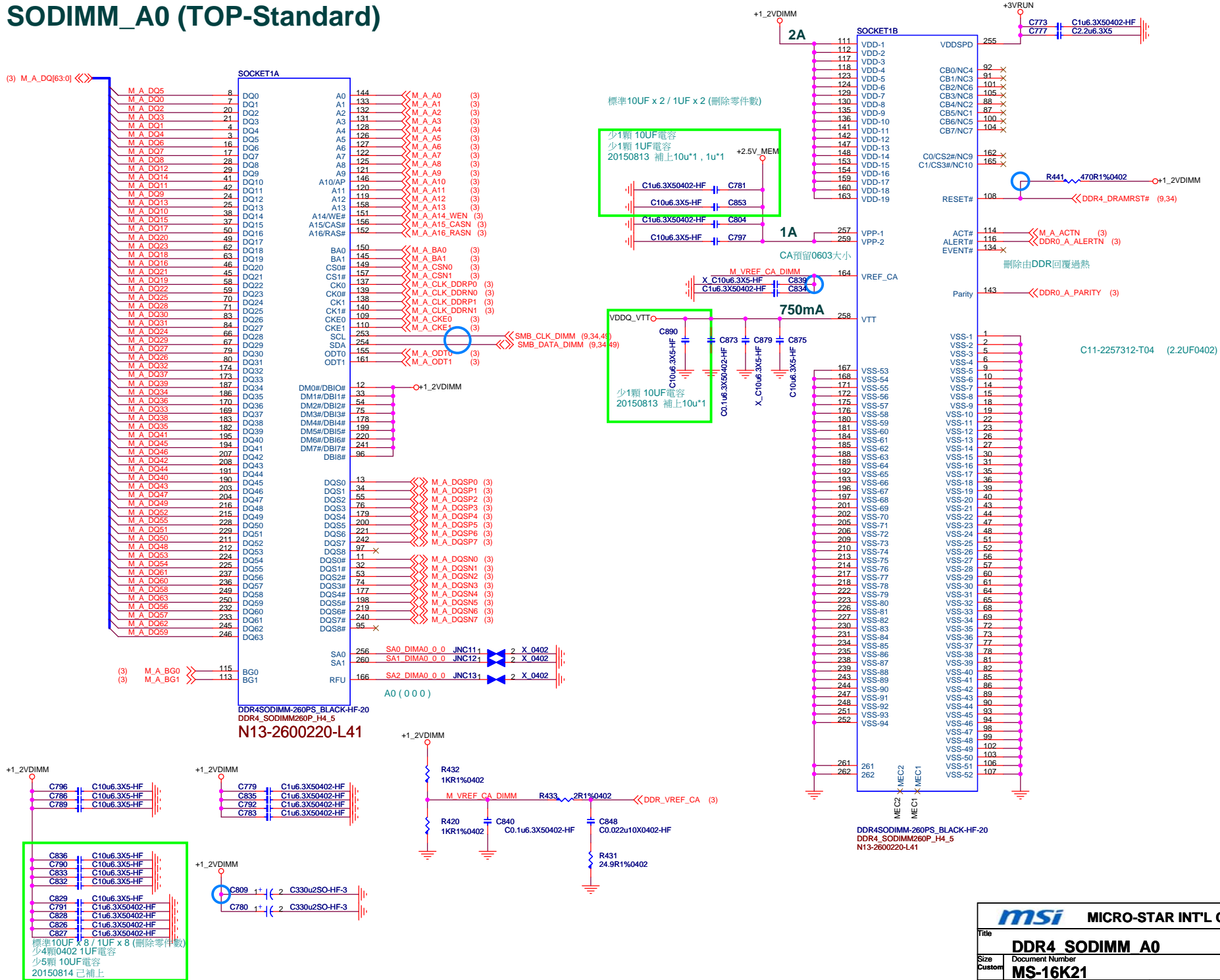




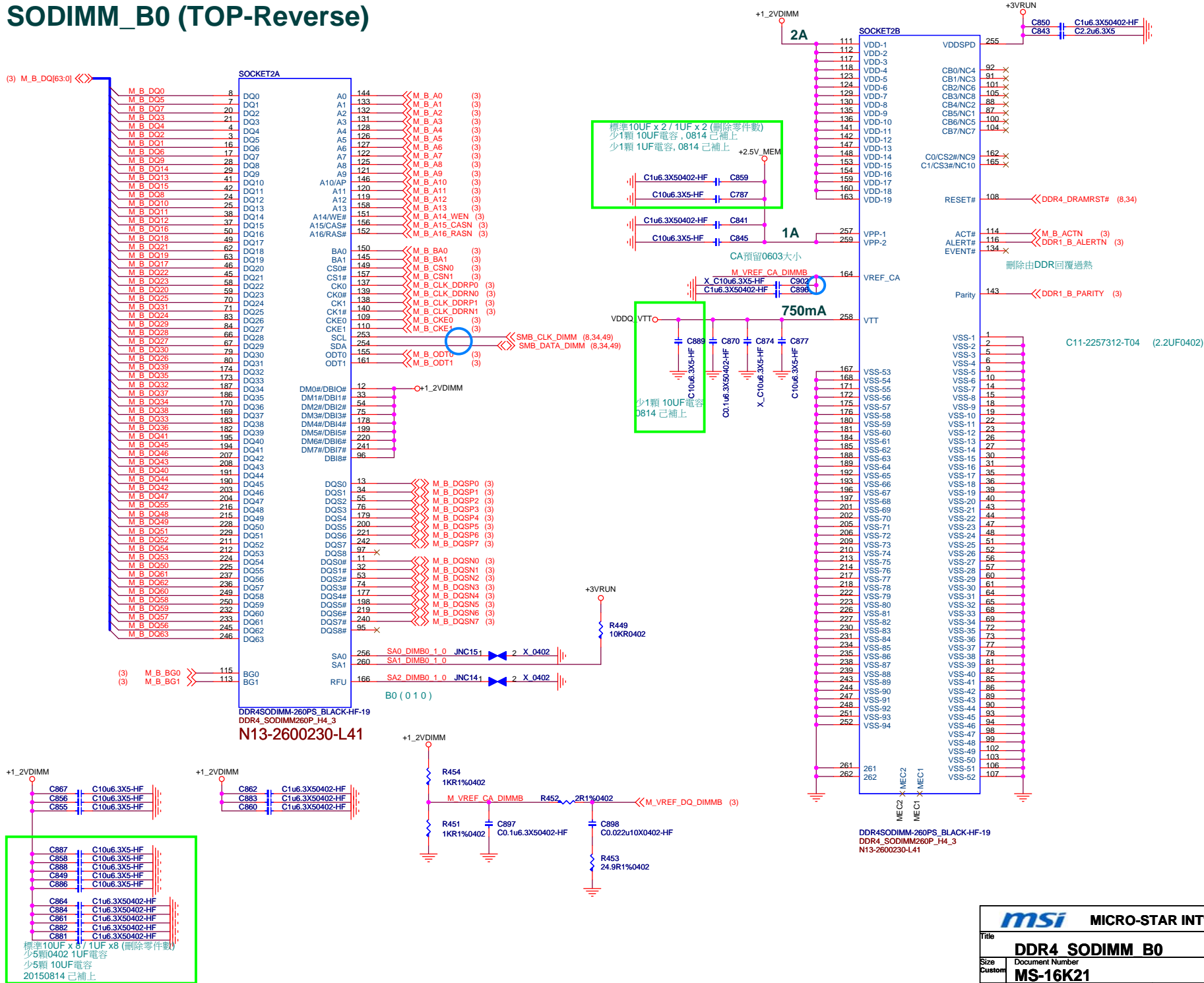




SODIMM_A0 (TOP-Standard)



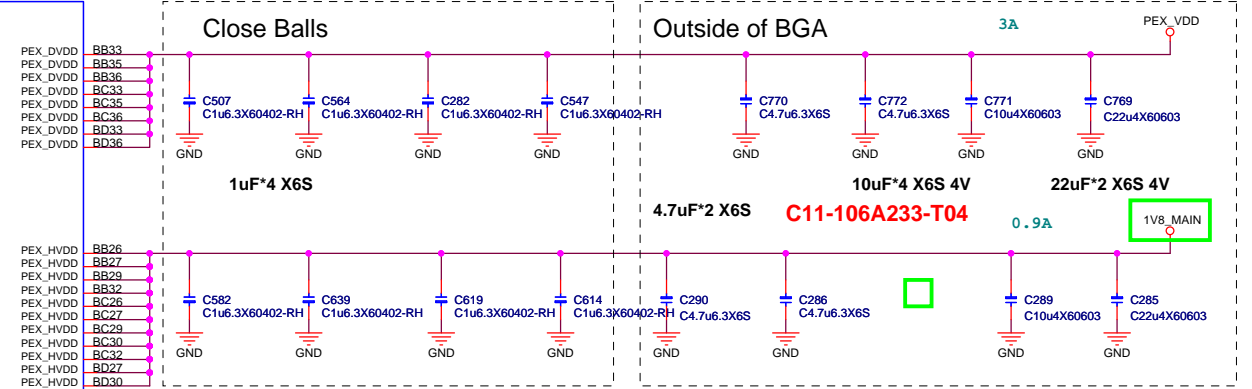
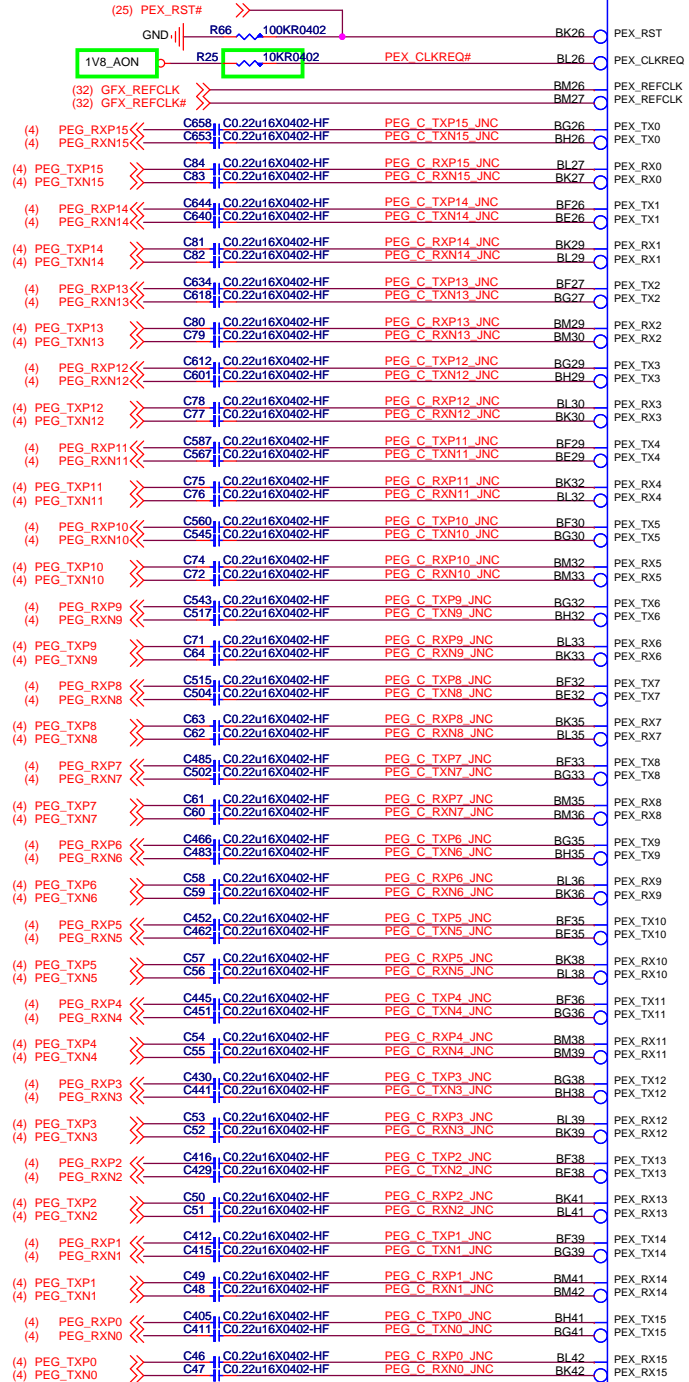
SODIMM_B0 (TOP-Reverse)



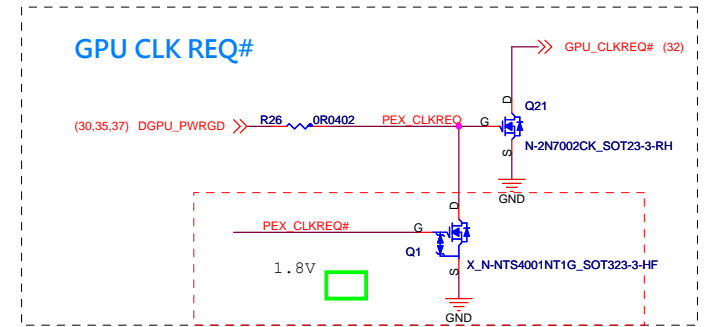
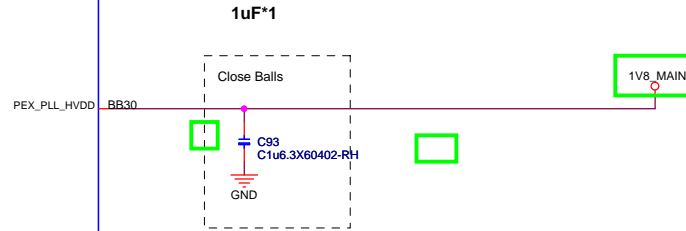
GPU PCI EXPRESS

G1A
INS7954024
BGA4152
COMMON

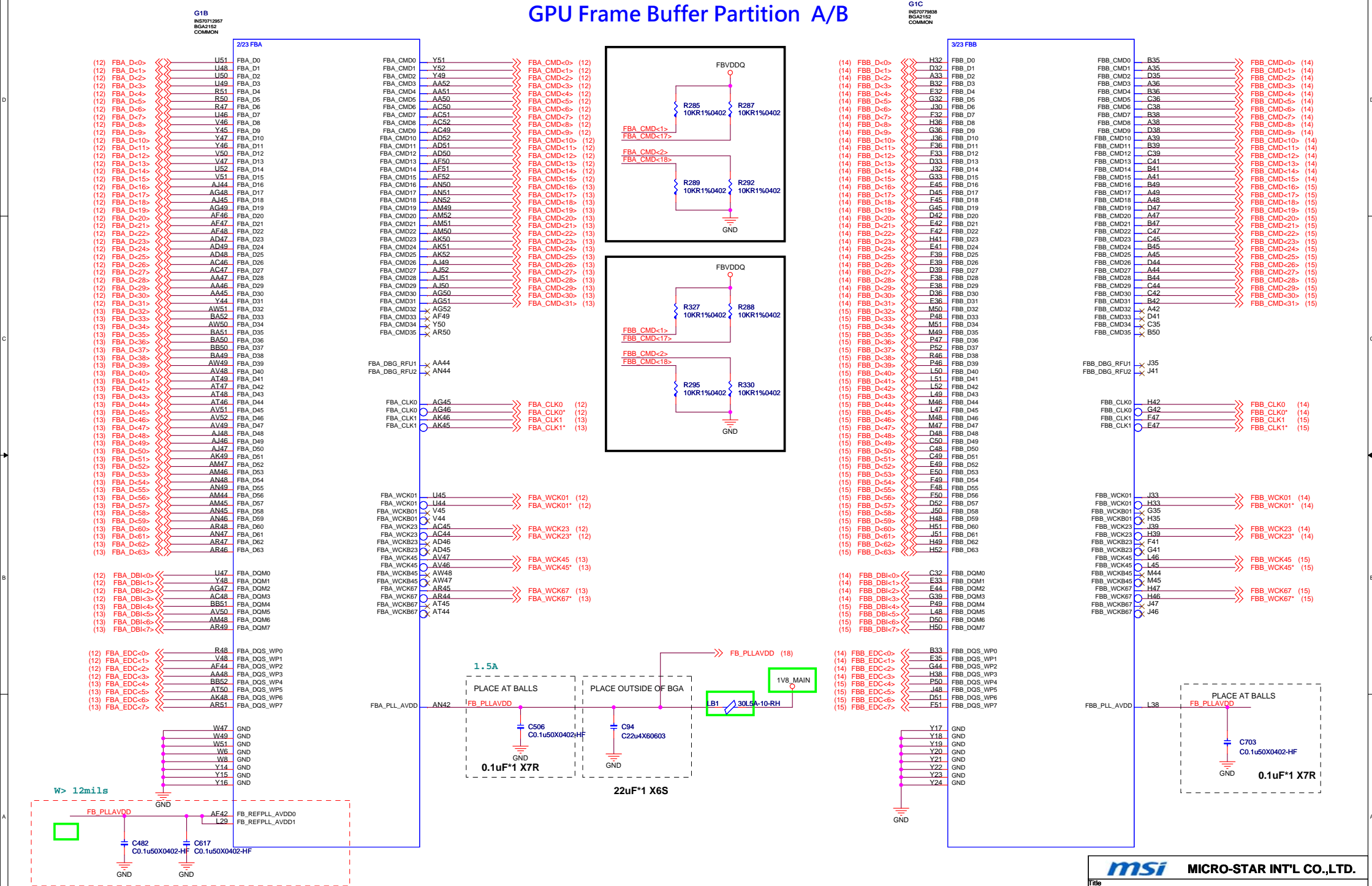
1/23 PCI_EXPRESS



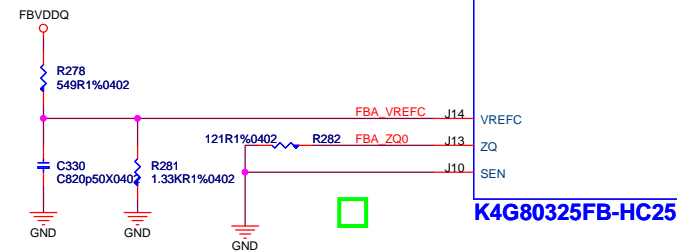
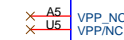
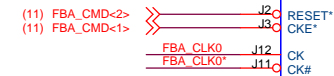
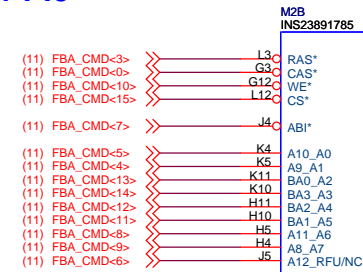
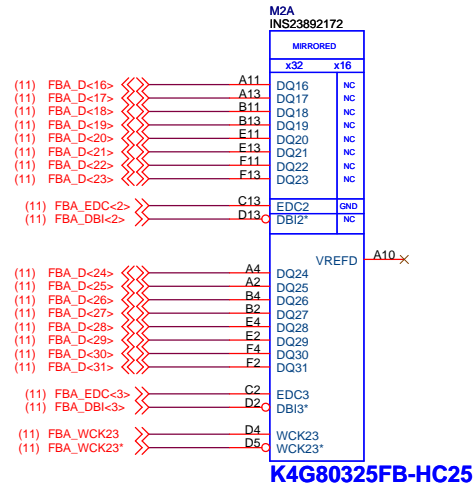
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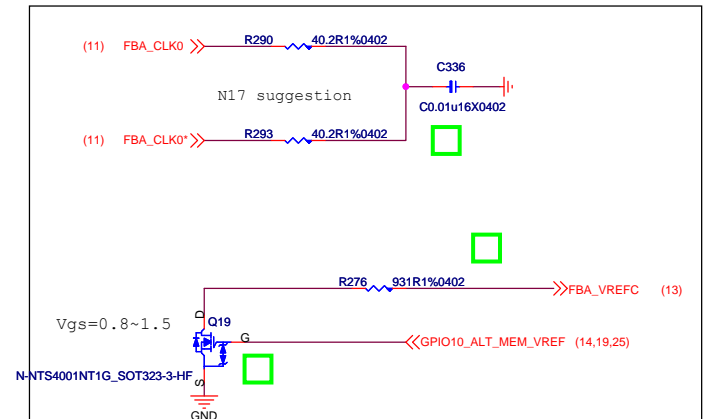
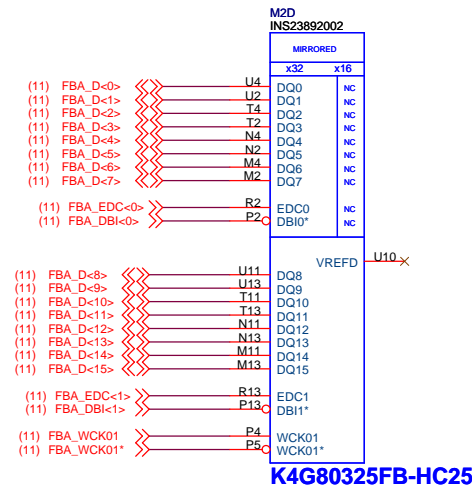
GPU Frame Buffer Partition A/B



DGPU_GDDR5 FrameBuffer A0

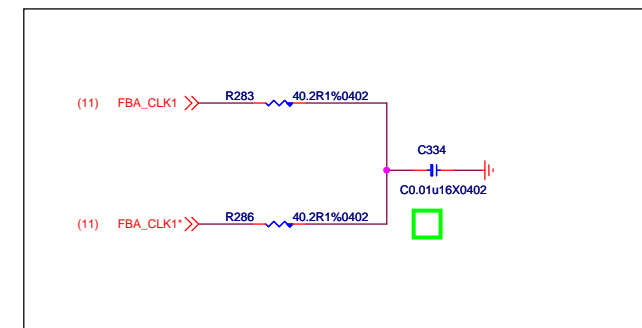
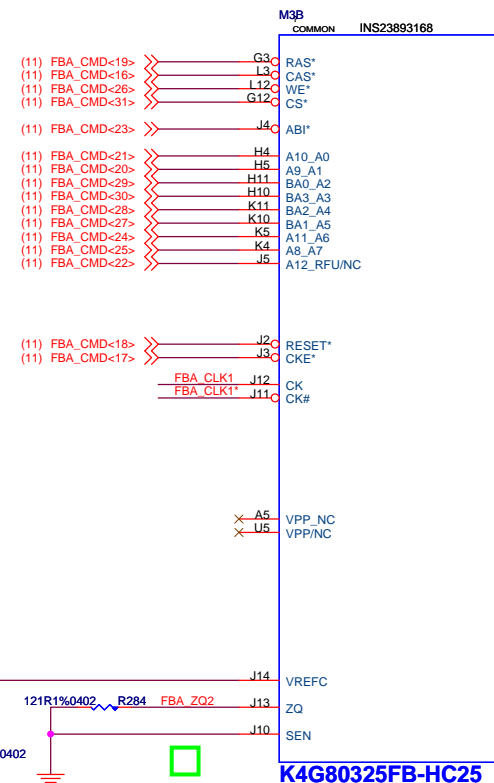
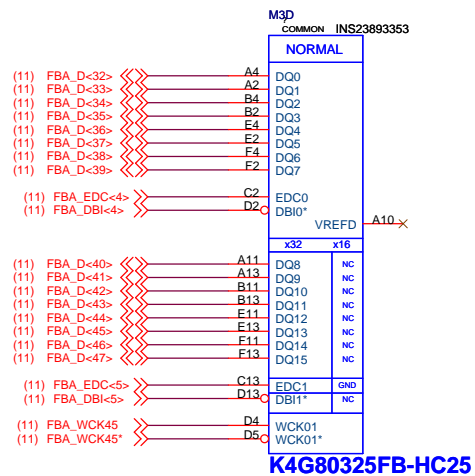
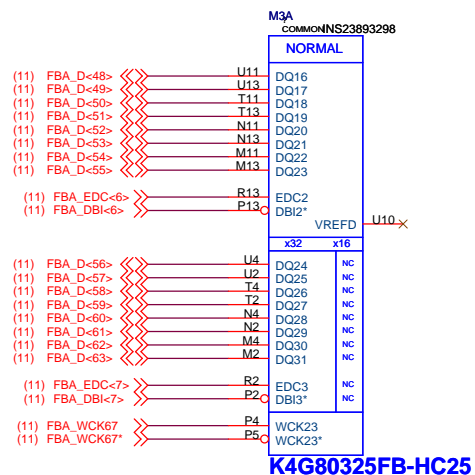


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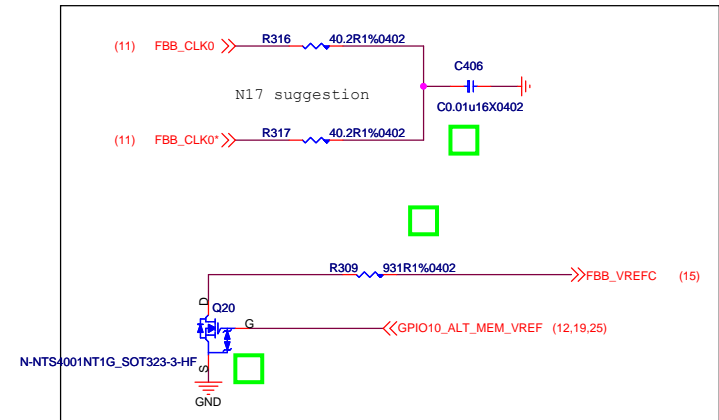
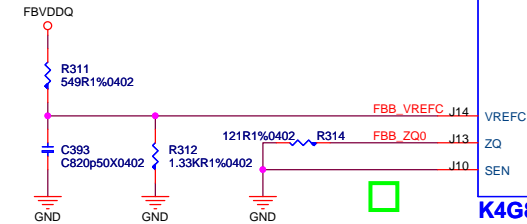
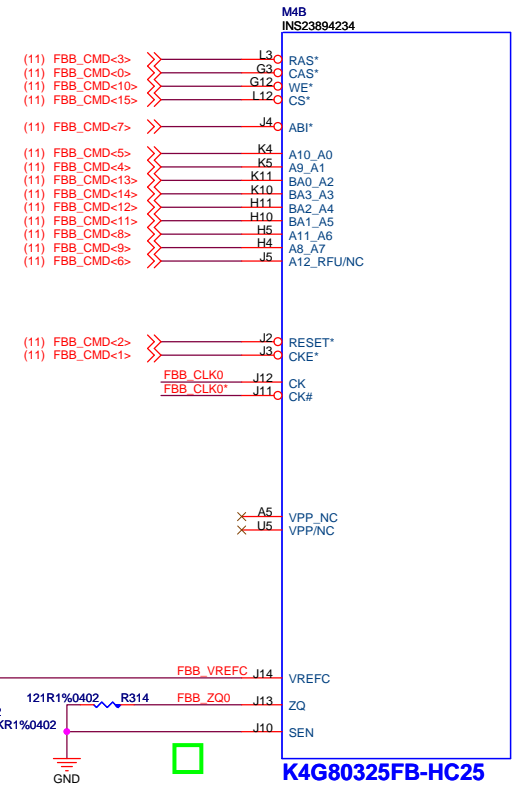
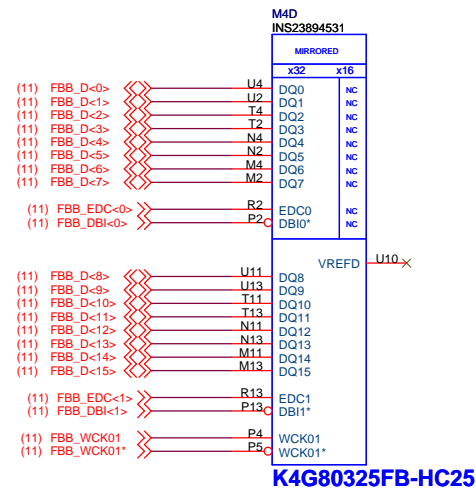
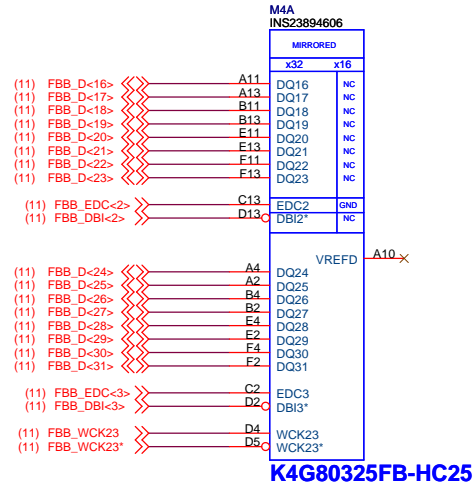


Hynix PN : M12-5GC2H05-H23 2G(64Mx32bit)
Samsung PN : M12-2032585-S02 2G(64Mx32bit)

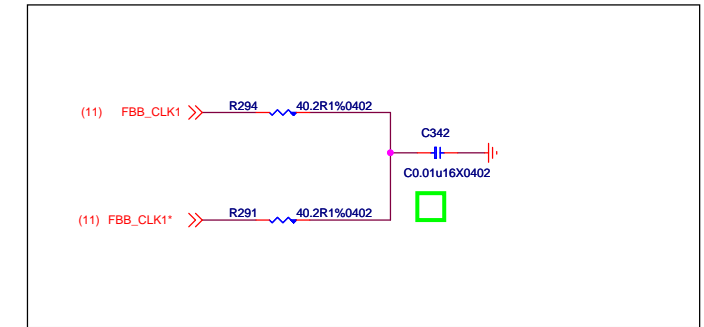
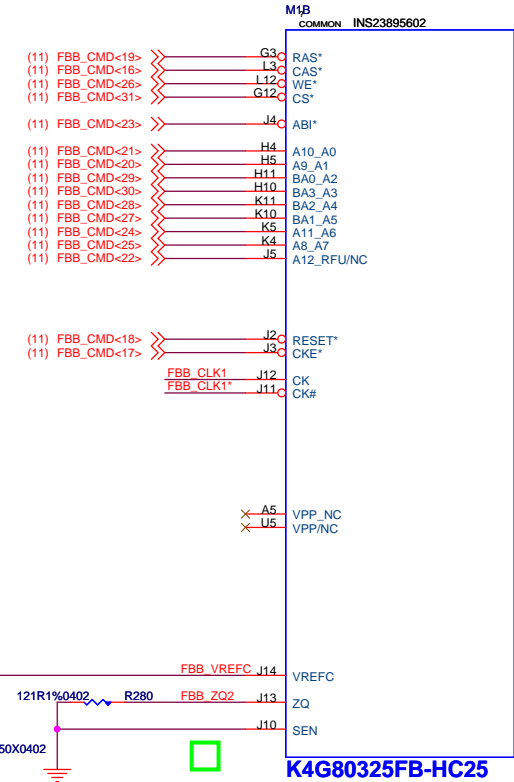
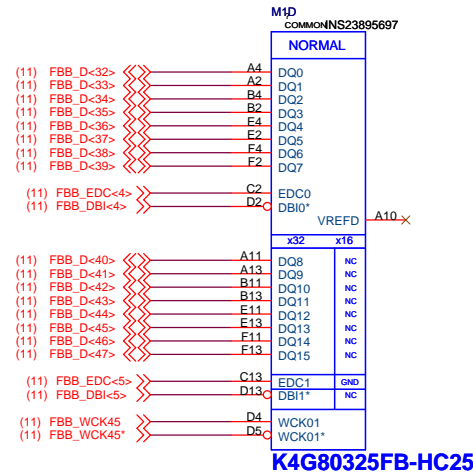
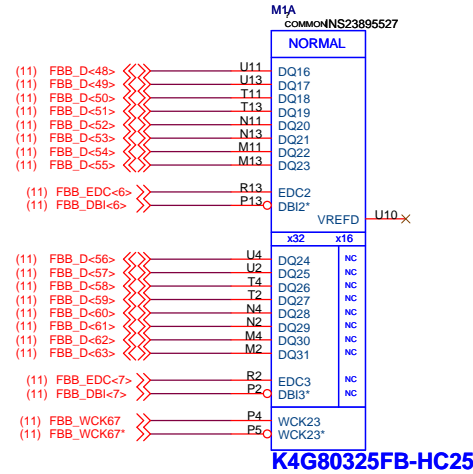
DGPU_GDDR5 FrameBuffer A1



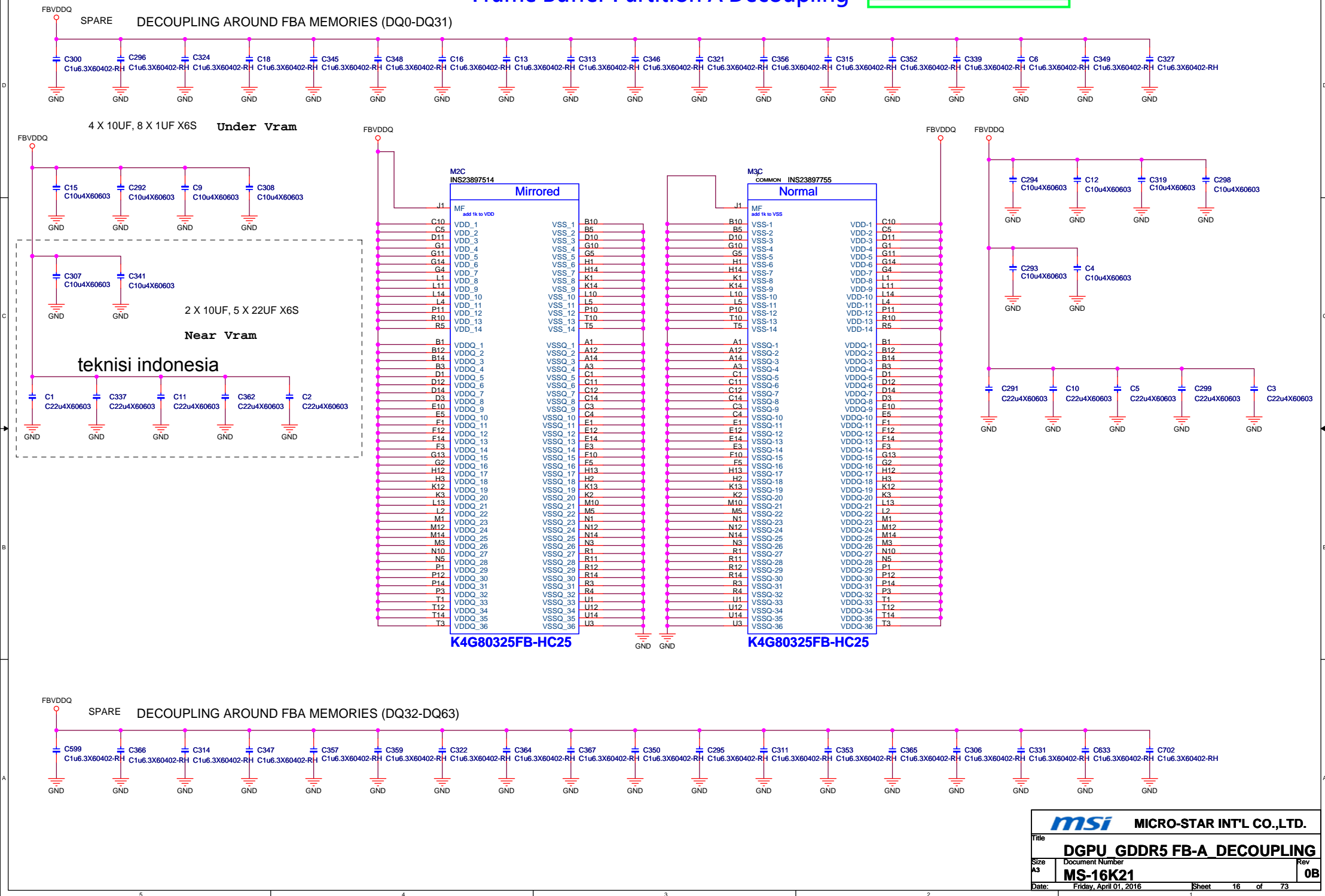
DGPU_GDDR5 FrameBuffer B0



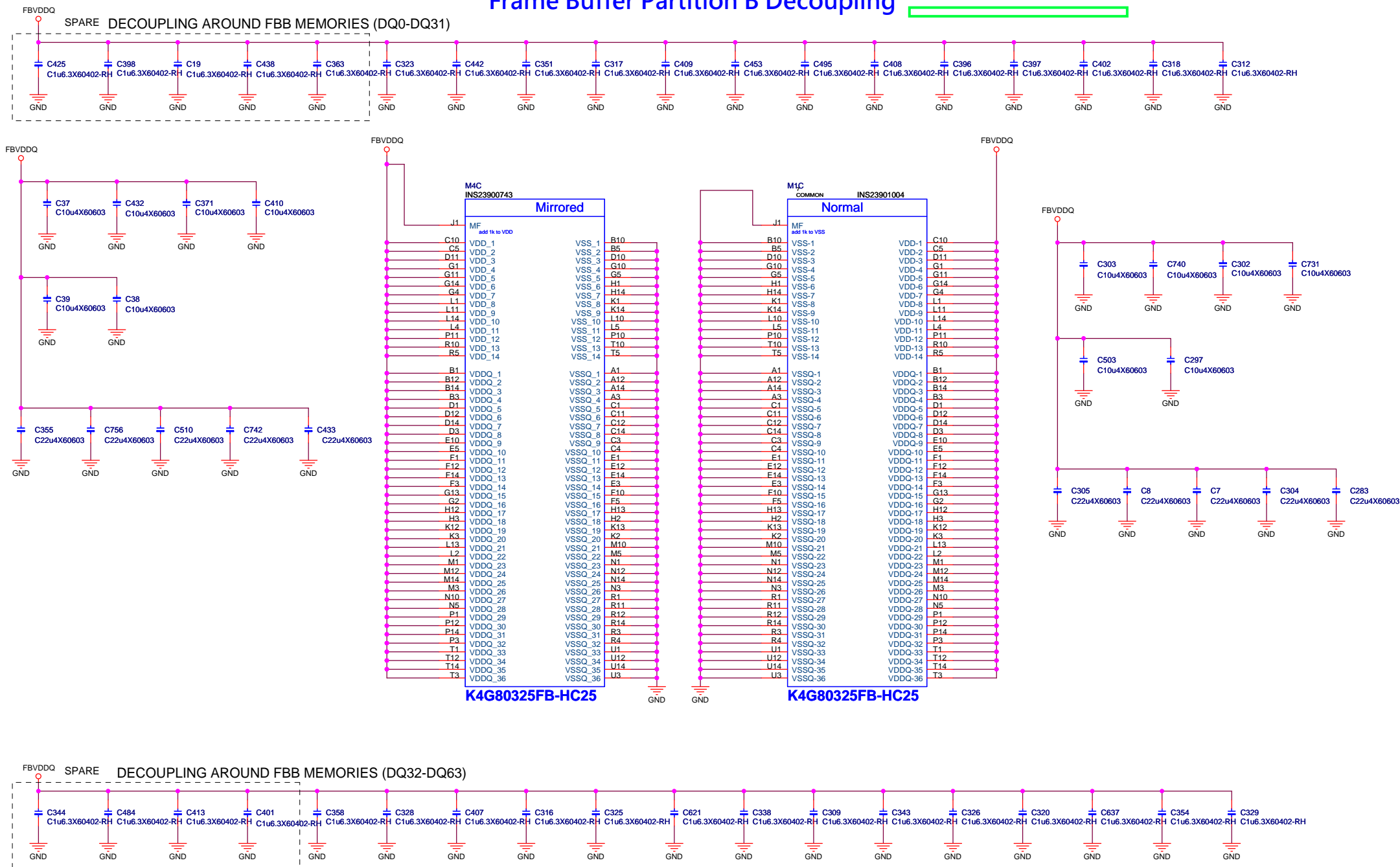
DGPU_GDDR5 FrameBuffer B1



Frame Buffer Partition A Decoupling



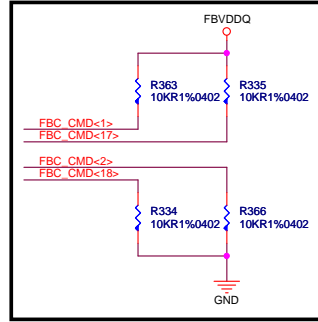
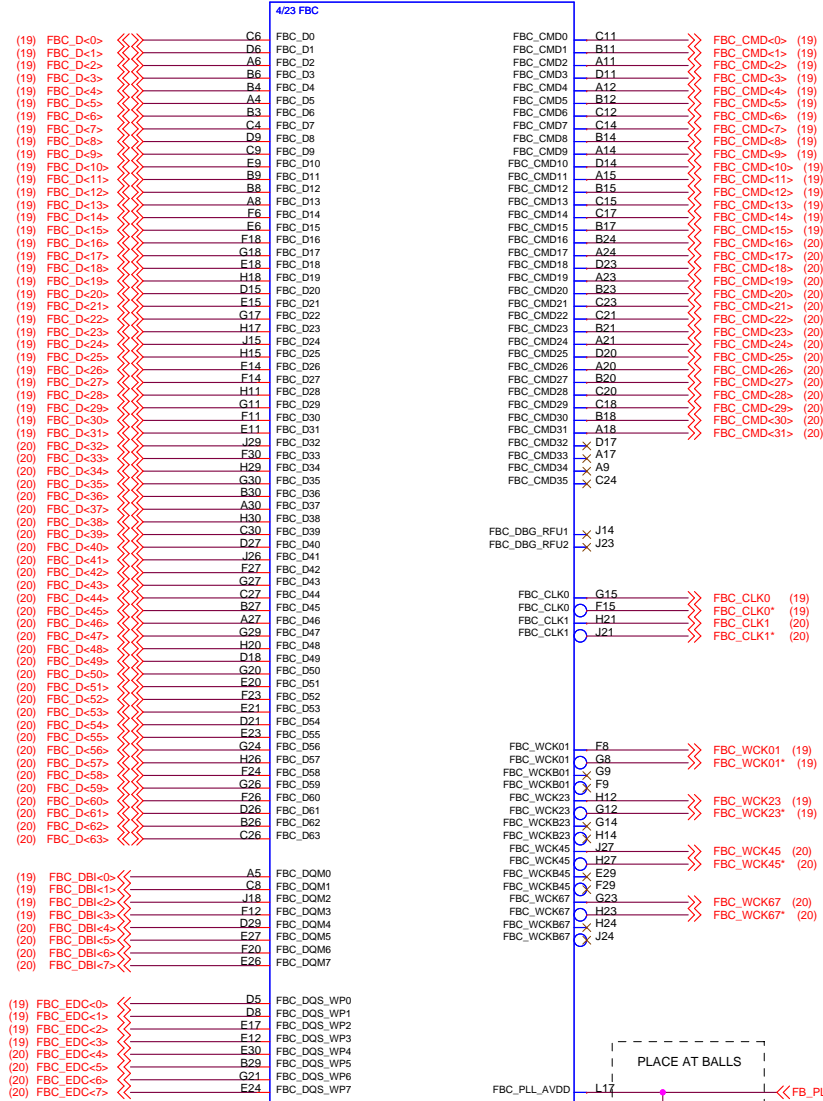
Frame Buffer Partition B Decoupling



GPU Frame Buffer Partition C/D

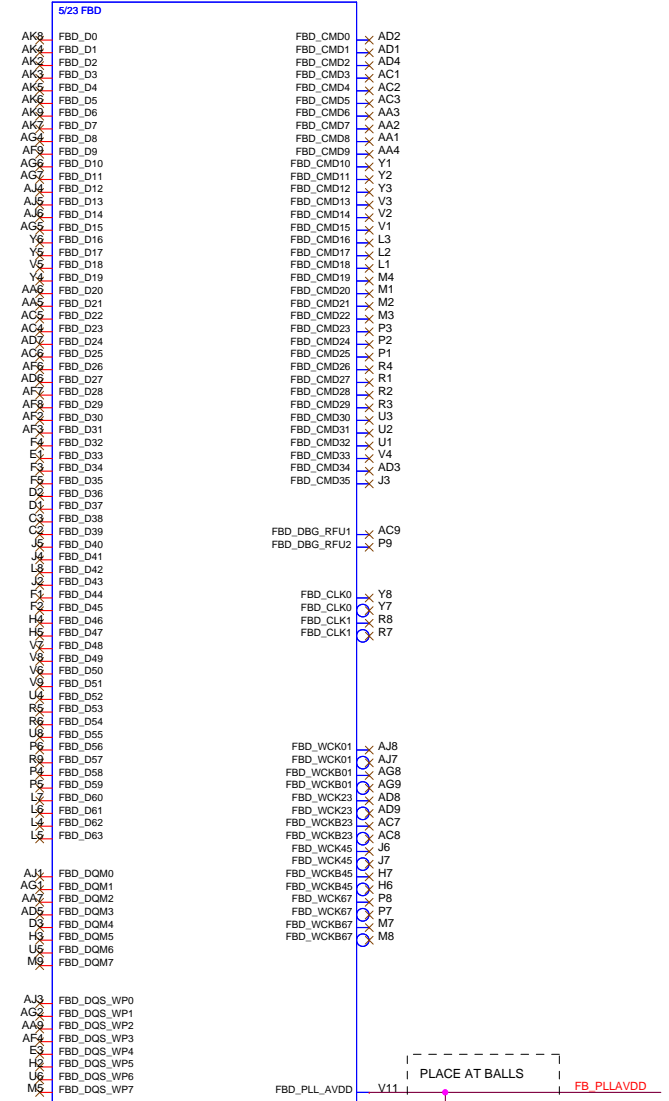
G1D
INS7080/7480
BGA2162
COMMON

G1E
INS7081/7481
BGA2162
COMMON



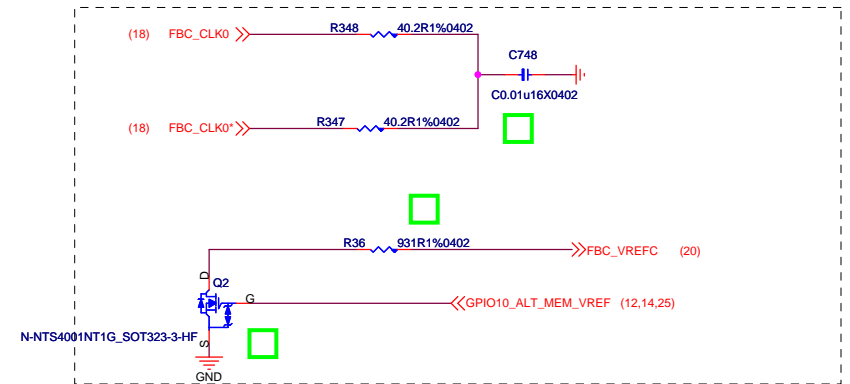
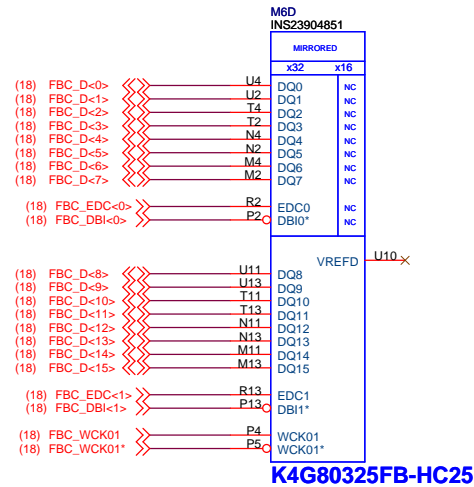
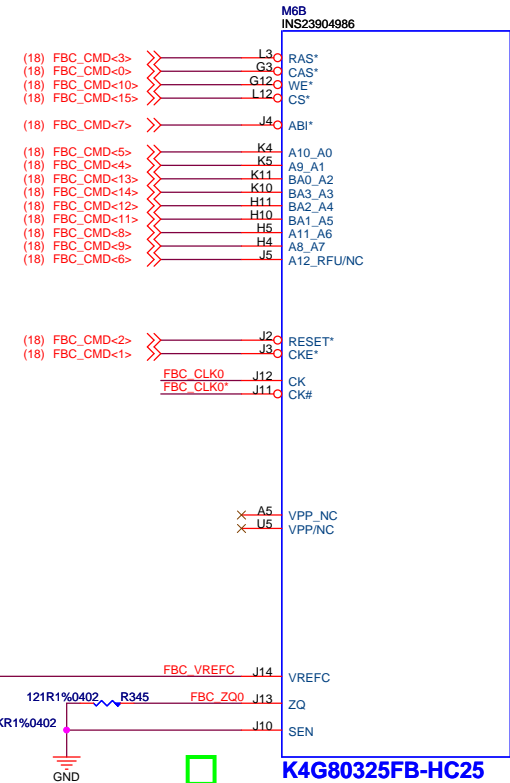
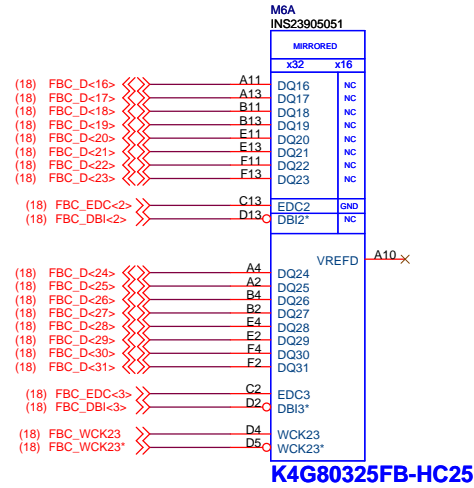
GDDR5 Mapping By GB4-256

	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1 A9	
CMD5	A0 A10	
CMD6	A12 RFU	
CMD7	AB1*	
CMD8	A6 A11	
CMD9	A7 A8	
CMD10	WF*	
CMD11	A5 BA1	
CMD12	A4 BA2	
CMD13	A2 BA0	
CMD14	A3 BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20	A1 A9	
CMD21	A0 A10	
CMD22	A12 RFU	
CMD23	AB1*	
CMD24	A6 A11	
CMD25	A7 A8	
CMD26	WF*	
CMD27	A5 BA1	
CMD28	A4 BA2	
CMD29	A2 BA0	
CMD30	A3 BA3	
CMD31	CS*	

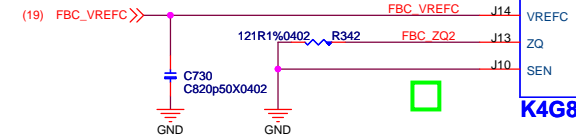
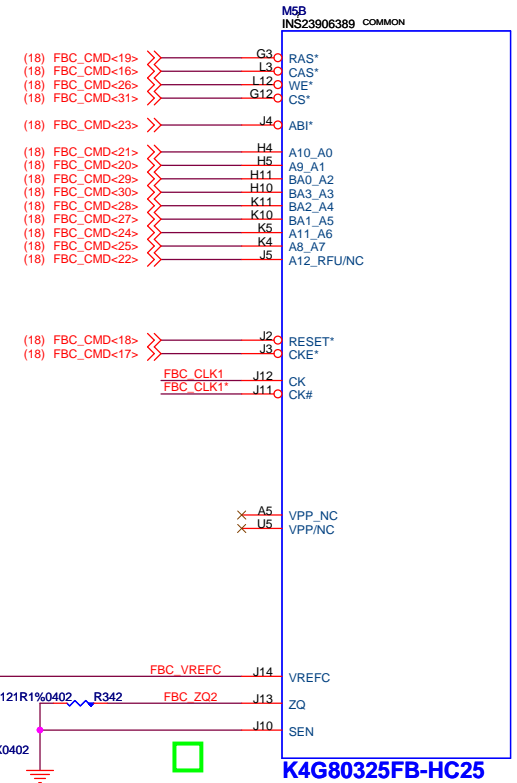
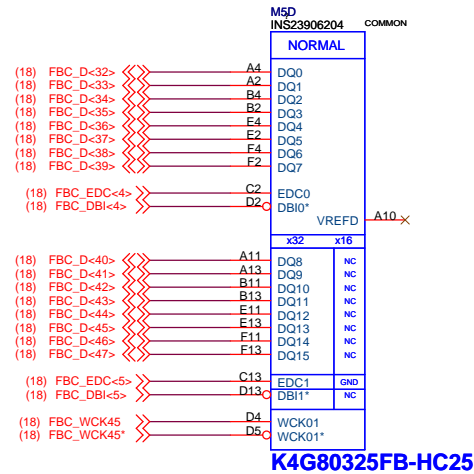
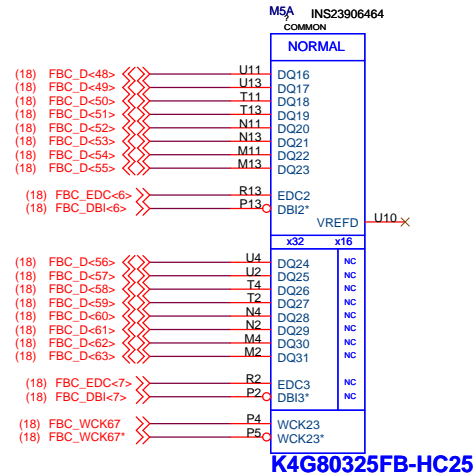


GP104
FBD
GP106
UNUSED

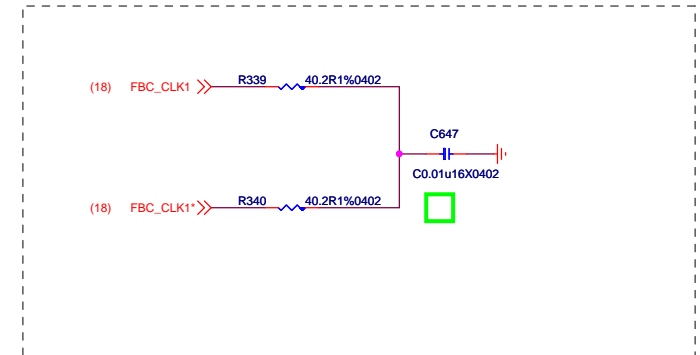
DGPU_GDDR5 FrameBuffer C0



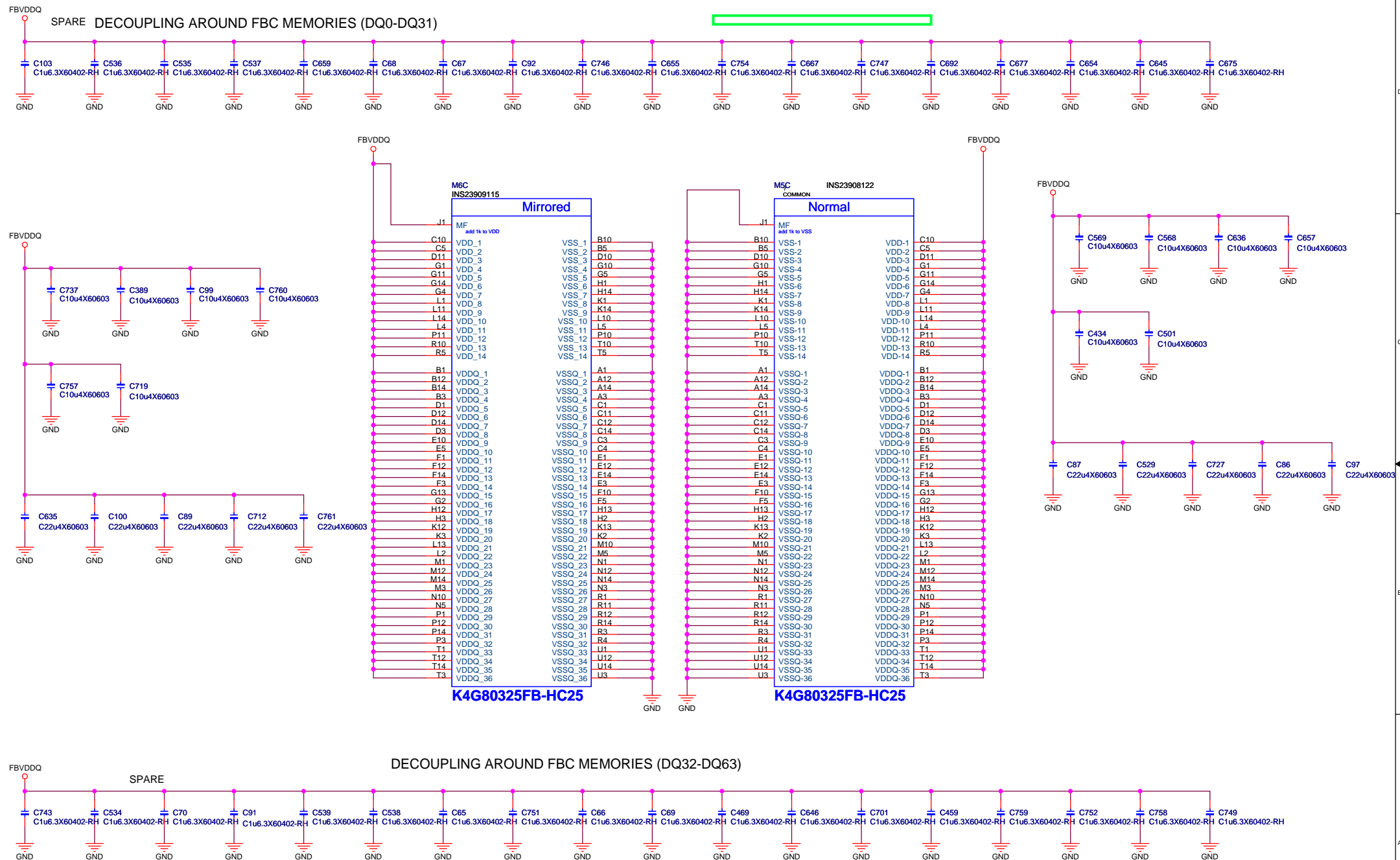
DGPU_GDDR5 FrameBuffer C1



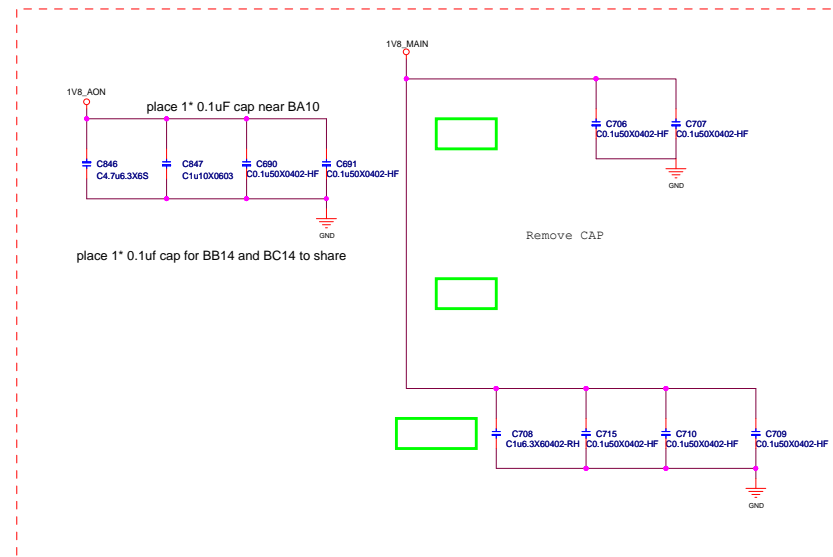
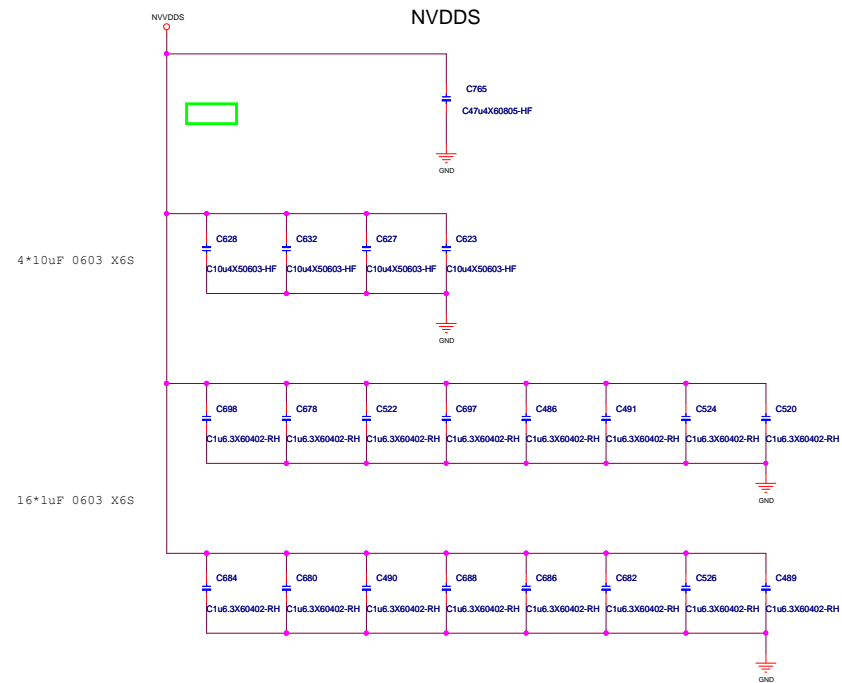
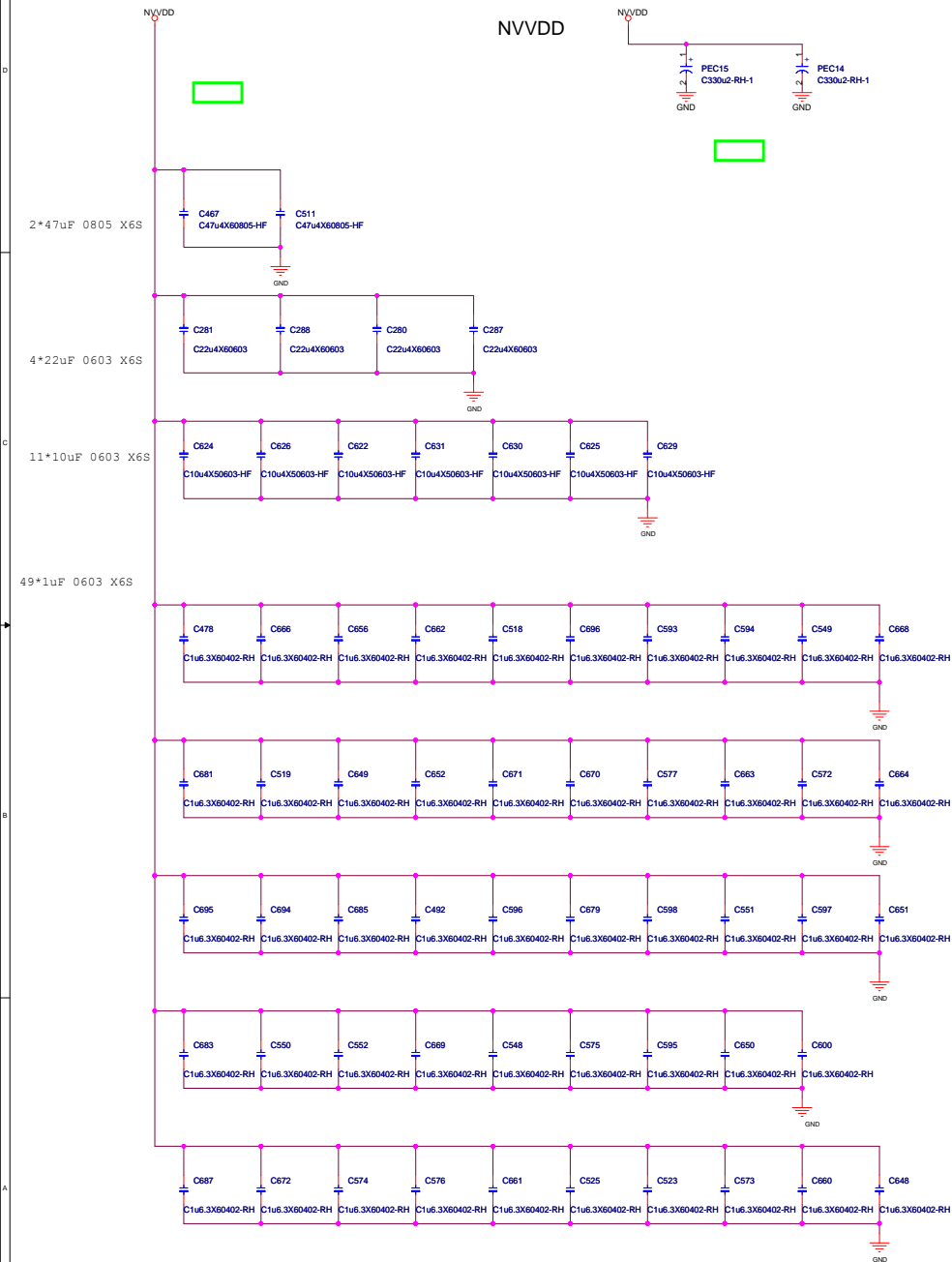
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Frame Buffer Partition C Decoupling

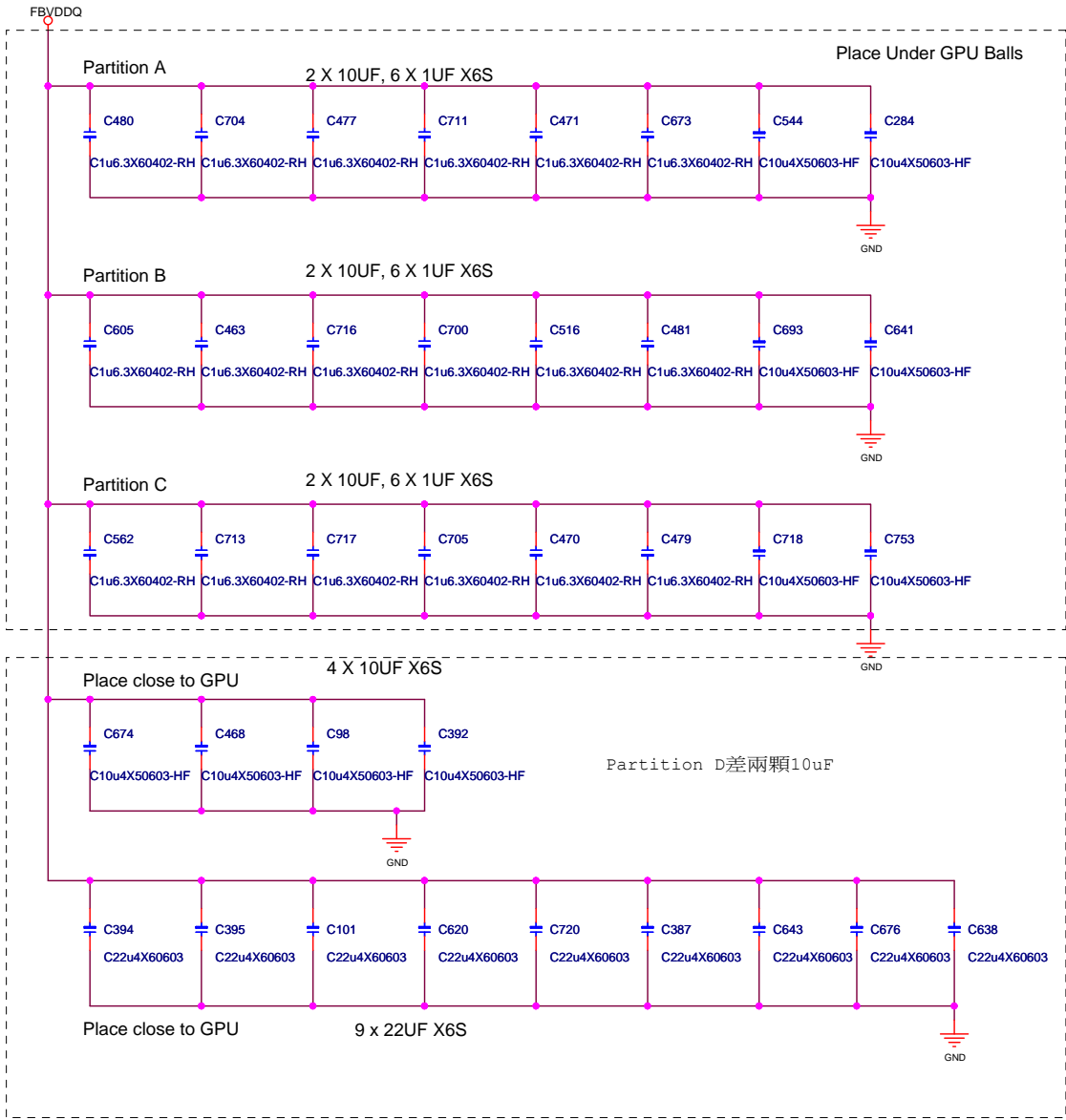


GPU DECOUPLING A

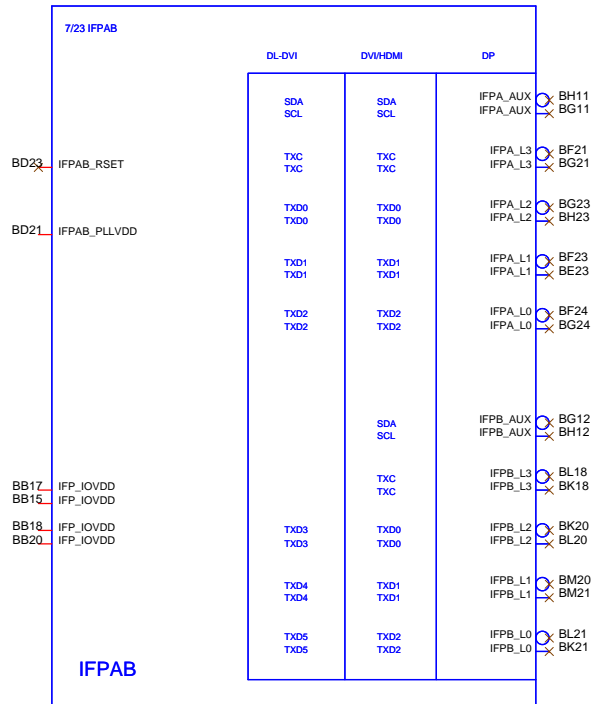


GPU DECOUPLING B

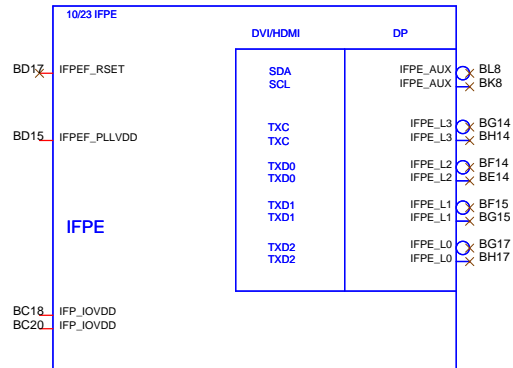
FBVDDQ



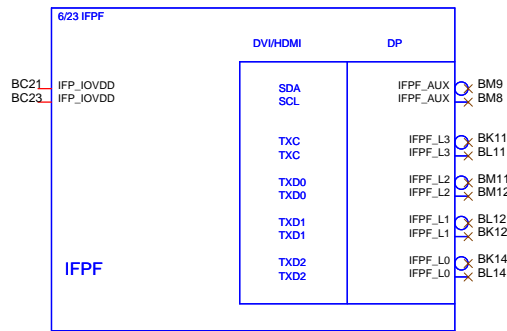
G1N
INST1468284
BGA2152
COMMON



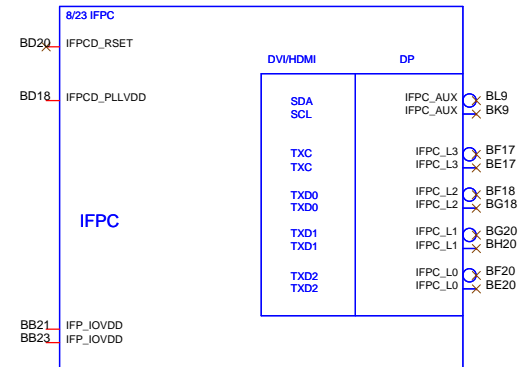
G1P
INST146825
BGA2152
COMMON



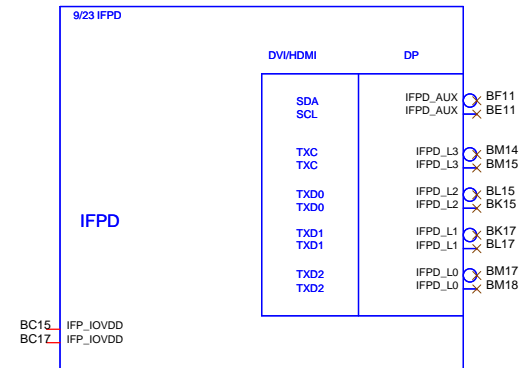
G1O
INST1468489
BGA2152
COMMON



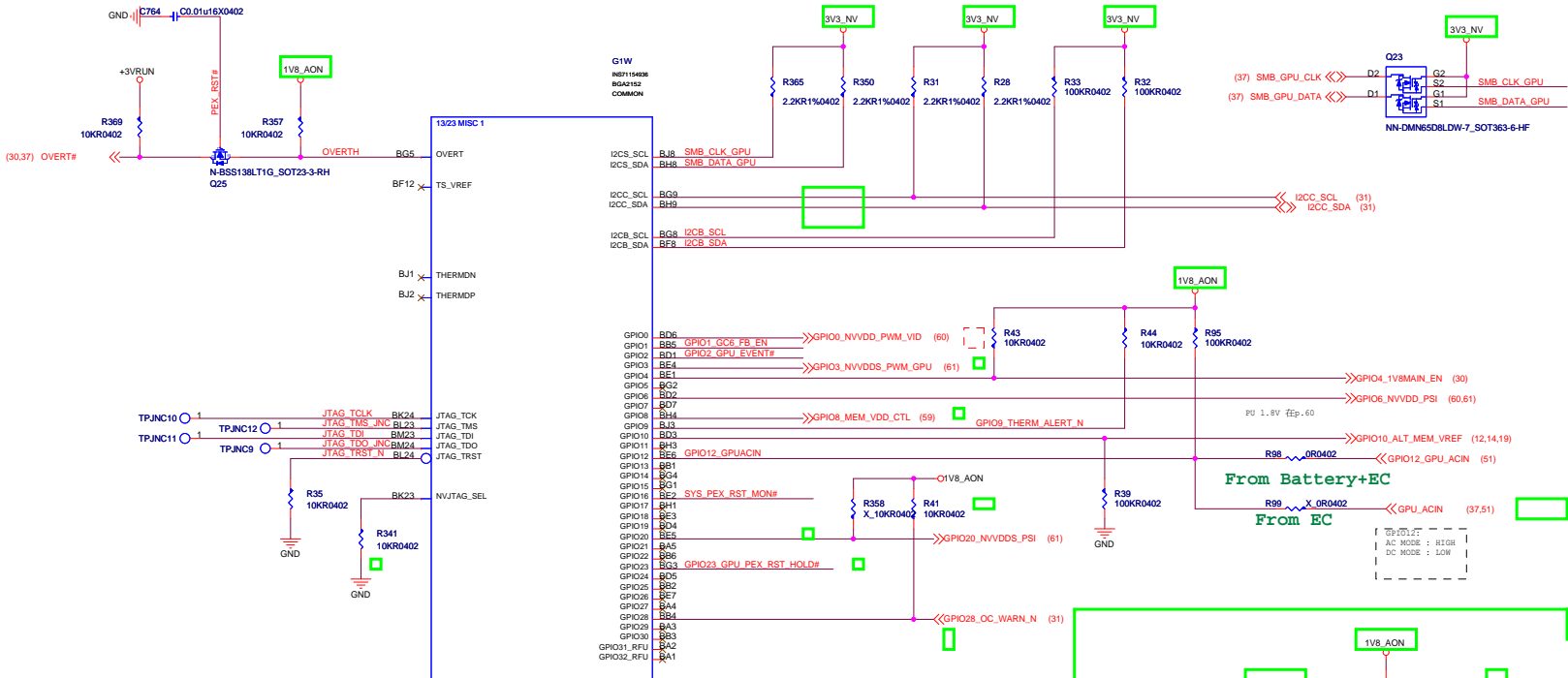
G1R
INST1468657
BGA2152
COMMON



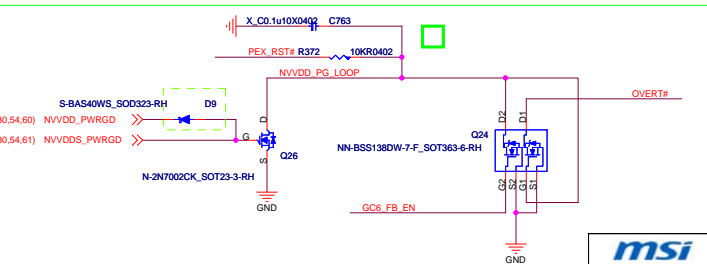
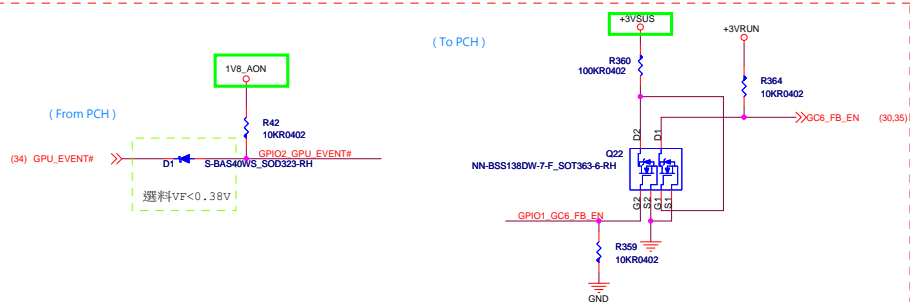
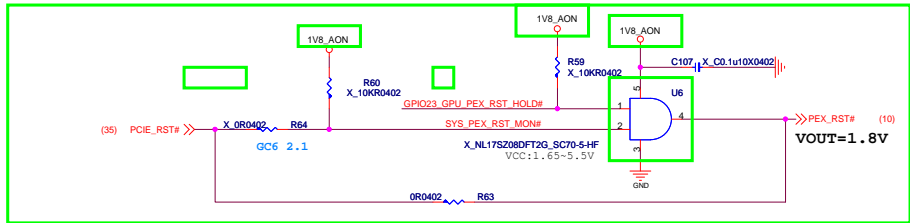
G1Q
INST1468795
BGA2152
COMMON



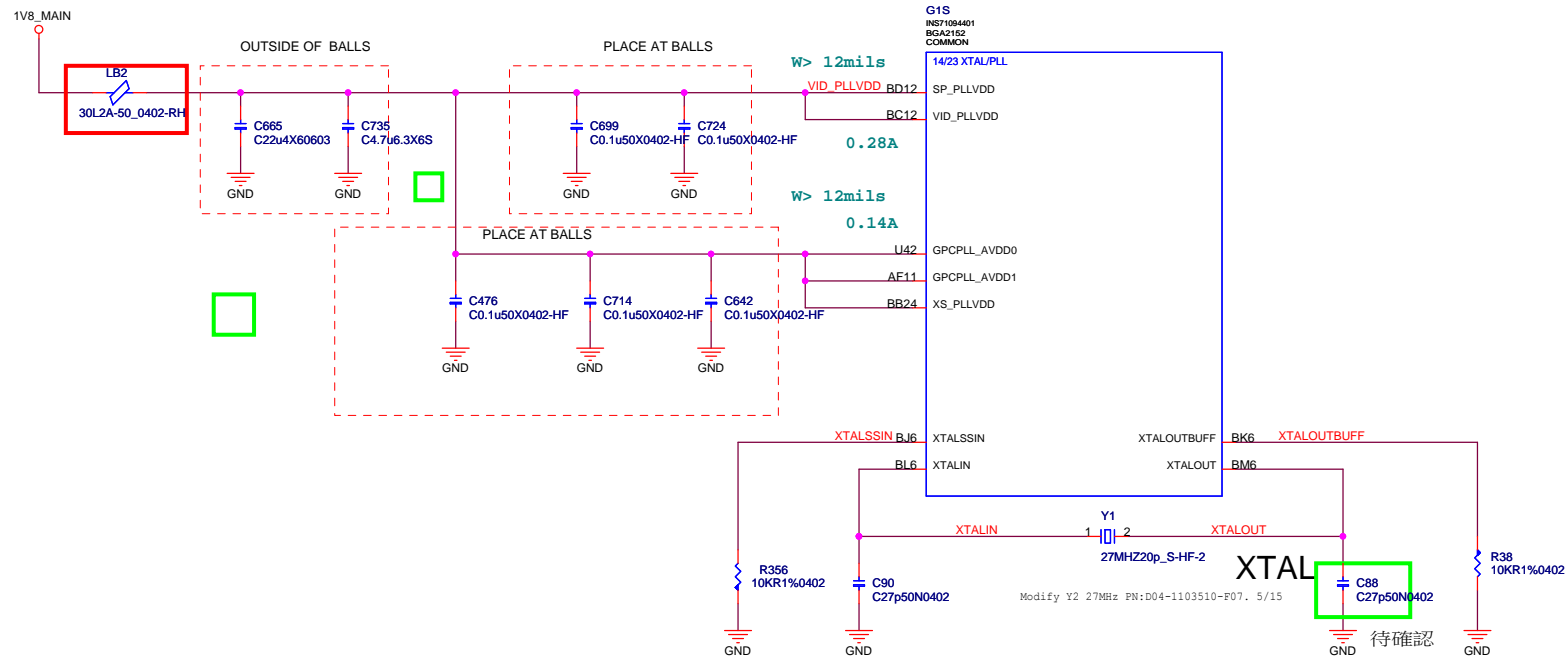
DGPU GPIO, I2C



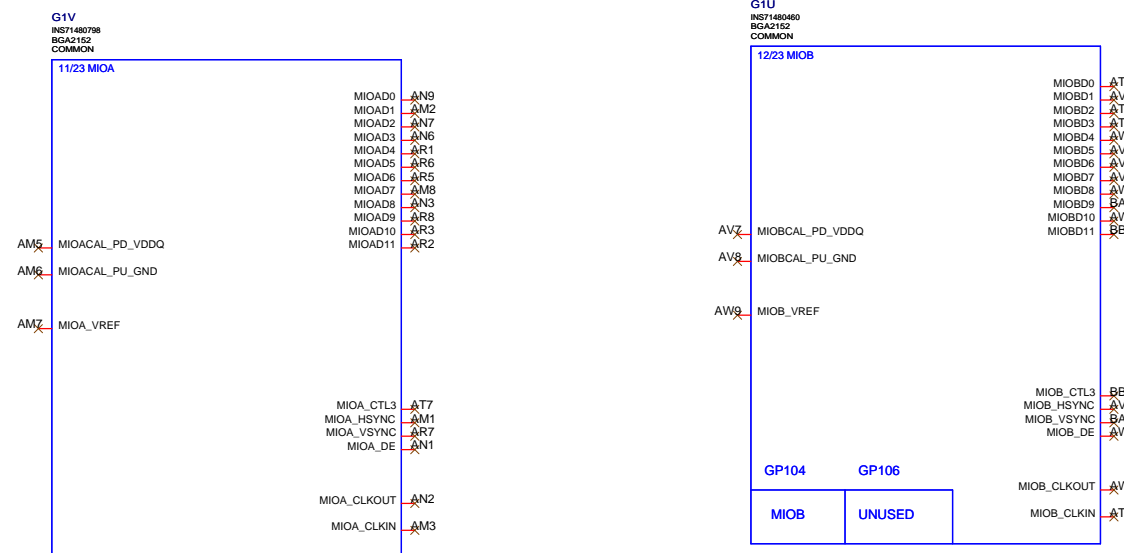
Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	PWR_VID	O	GPU Core VDD PWM control signal	0 to 1V8 PWM output
GPIO1	GC6_FB_EN	O	FB Enable for GC6 2.1	10K pull-down
GPIO2	GPU_EVENT#	I	GPU wake signal for GC6 2.1	10K pull-up to 1V8_AON
GPIO3	NVVDD_SRAM_PWM	O	PWM output to control the SRAM power supply	
GPIO4	1V8_MAIN_EN	O	GPU POWER Sequencing for GC6 2.1	10K pull-up to 1V8_AON
GPIO5	FRM_LCK	I	Active low Fram Lock	1V8 pull-up to 1V8_AON
GPIO6	PSI	O	Phase shedding	10K pull-up to 1V8_AON
GPIO7	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO8	MEM_VDD_CTL	O	Memory Voltage Control	pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	10K pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VCC	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO14	HPD_A	I	Hot Plug Detect for IFPA	
GPIO15	HPD_B	I	Hot Plug Detect for IFPB	
GPIO16	SYS_PEX_RST_MON#	I	System side PCI reset Monitor	10K pull-up to 1V8_AON
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	
GPIO19	3DVision	O	3D Vision L/R signal	100K pull-down
GPIO20	NVVDDS_PSI GC5_MODE	O		
GPIO21	SLI_RASTER_SYNC	I	SLI Raster Sync	100K pull-down
GPIO22	SLI_SWAP_DRY	I	SLI Swap Ready	
GPIO23	GPU_PEX_RST_HOLD	O	GPU PCIe self-reset control	OD 10K pull-up to 3V3
GPIO24	HPD_F	I	Hot Plug Detect for IFPDF	
GPIO25	RESERVED			
GPIO26	RESERVED			
GPIO27	HPD_C	I	Hot Plug Detect for IFPC	
GPIO28	OC_WARN	I	Over current throttling	10K pull-up to 1V8_AON
GPIO29	EDPc_OUTPUT_CAP	I	Input from power supply	0 to 1V8
GPIO30	RESERVED			



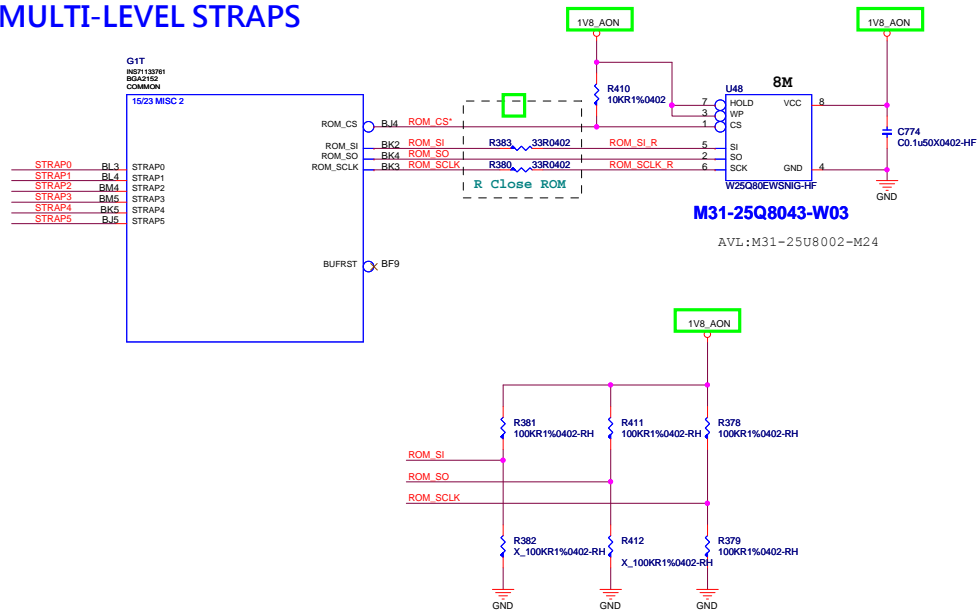
DGPU MIO & XTAL



Multi-use IO(MIO) Interface



ROM, MULTI-LEVEL STRAPS



STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	V
L	L	H	00001	V
L	H	L	00010	
L	H	H	00011	
H	H	L	00110	
H	H	H	00111	

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

SAMSUNG 0X0
MICRON 0X1
HYNIX 0X2

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	V

SOR_EXPOSED :GPU AUDIO SETTING

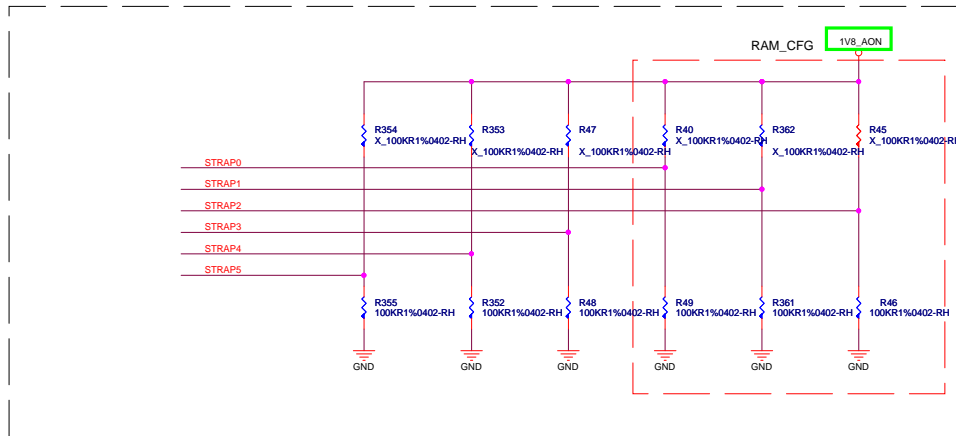
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0 V

1:SMB_ALT_ADDR ENABLE (DUAL GPU)
0:SMB_ALT_ADDR DISABLE (SINGLE GPU)

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

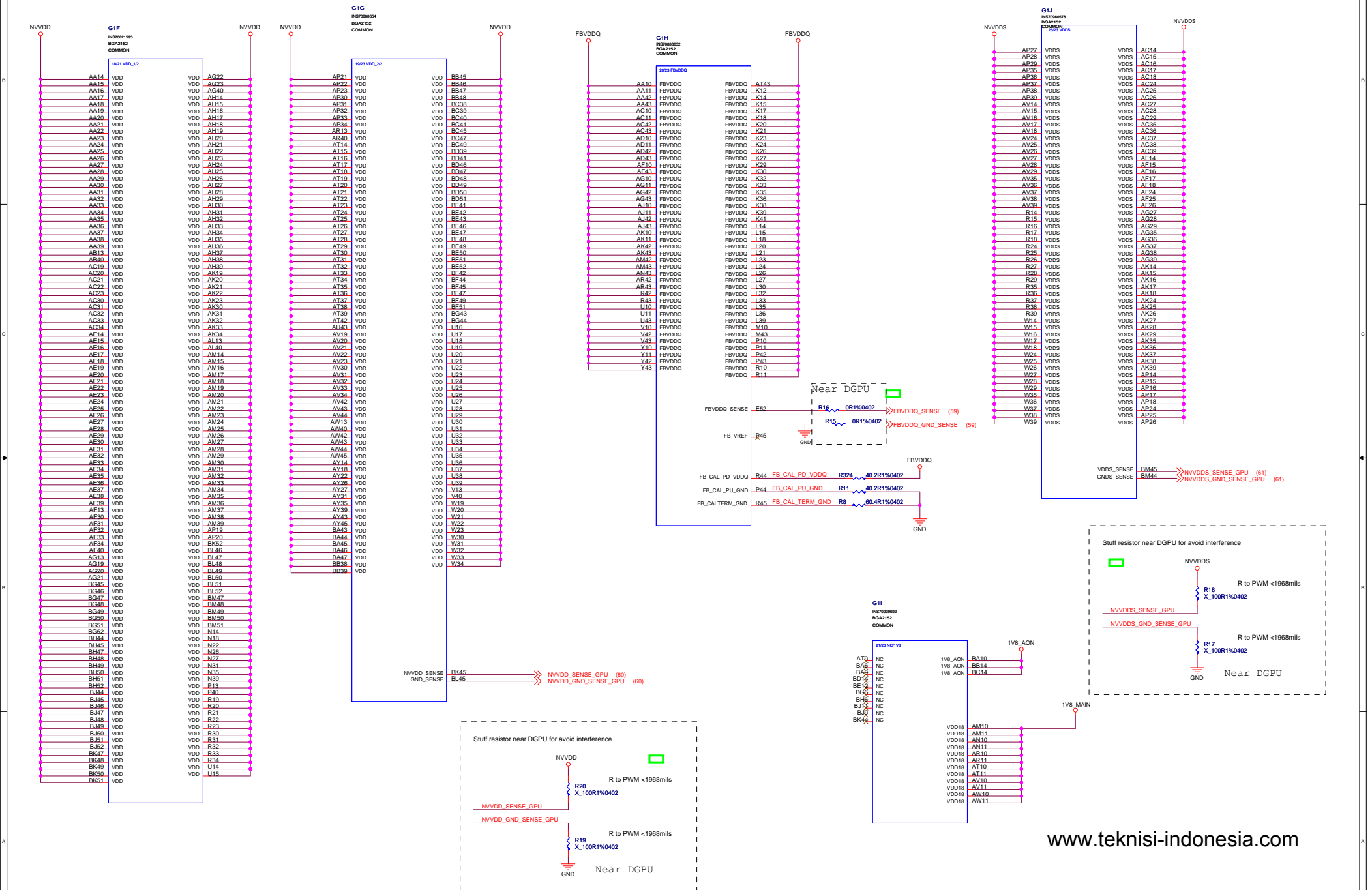
1:PCIE_CFG LOW SWING POWER
0:PCIE_CFG HIGH SWING POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



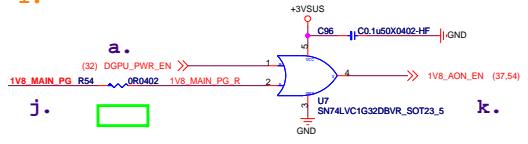
DEFAULT SETTING	<input checked="" type="checkbox"/> 5010
	M12-8032535-S02
	X_K4G80325FB-HC25
V_TOP2	<input checked="" type="checkbox"/> 5010
	M12-2563215-M30
	X_MT51J256M32HF-80:A
V_TOP3	<input checked="" type="checkbox"/> 5010
	M12-5GC2H05-H23
	X_H5GC2H24BFR-T2C

GPU NVVDD, FBVDDQ

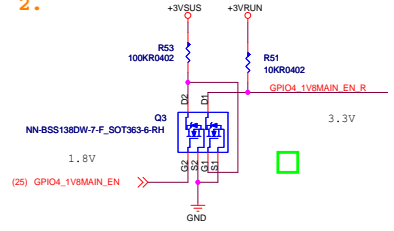


nVIDIA Power Sequence Control Power on = 1V8_AON -> 1V8_MAIN -> 3V3_NV -> NVVDD -> NVVDDS/PEX_VDD -> FBVDDQ -> DGPUPWRGD
Power off = DGPUPWREN -> (NVVDDS -> PEX_VDD -> FBVDDQ) -> (NVVDD -> 3V3_NV) -> 1V8_MAIN -> 1V8_AON

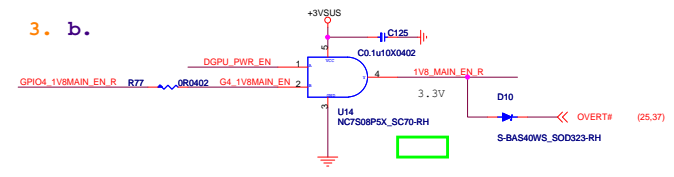
1.



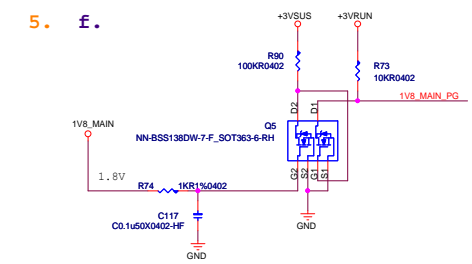
2.



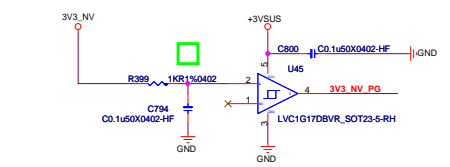
3. b.



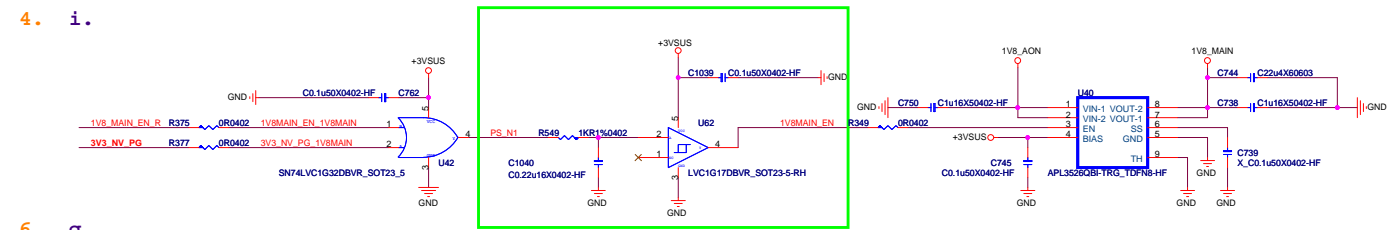
5. f.



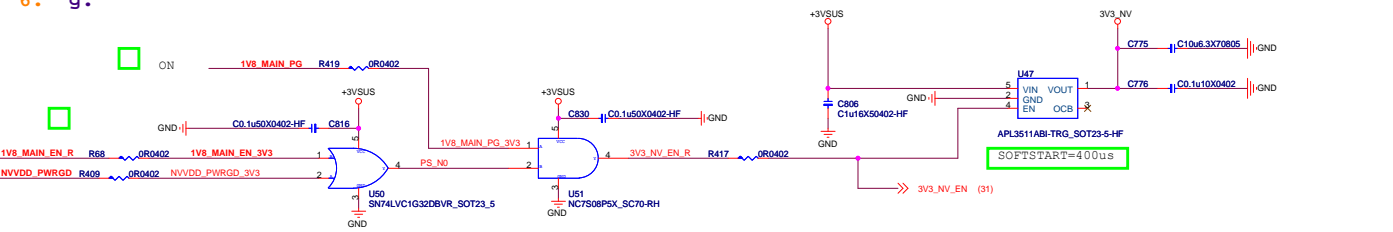
7. h.



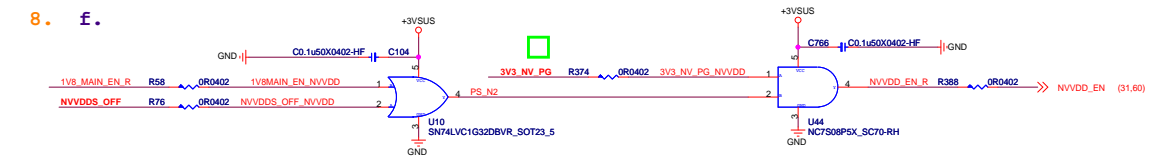
4. i.



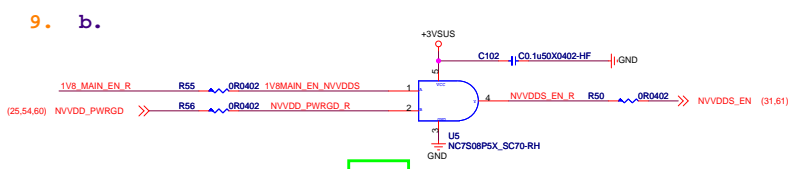
6. g.



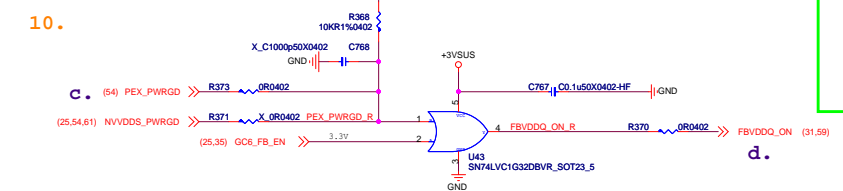
8. f.



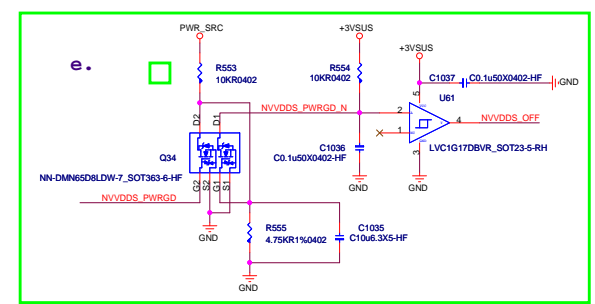
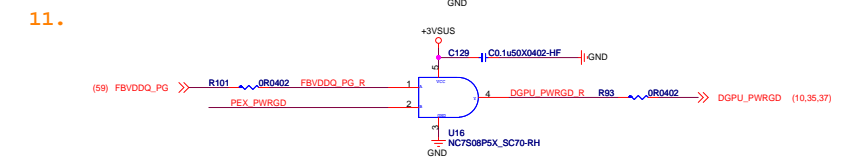
9. b.



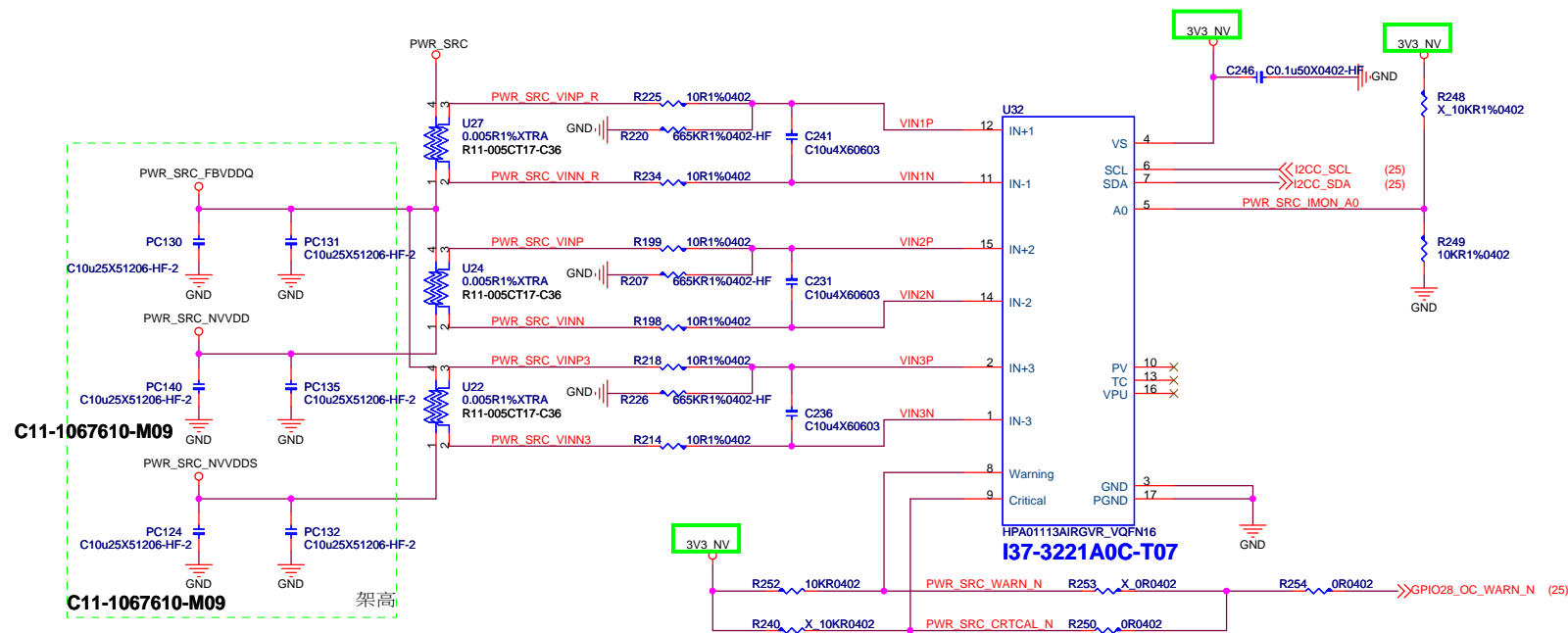
10.



11.

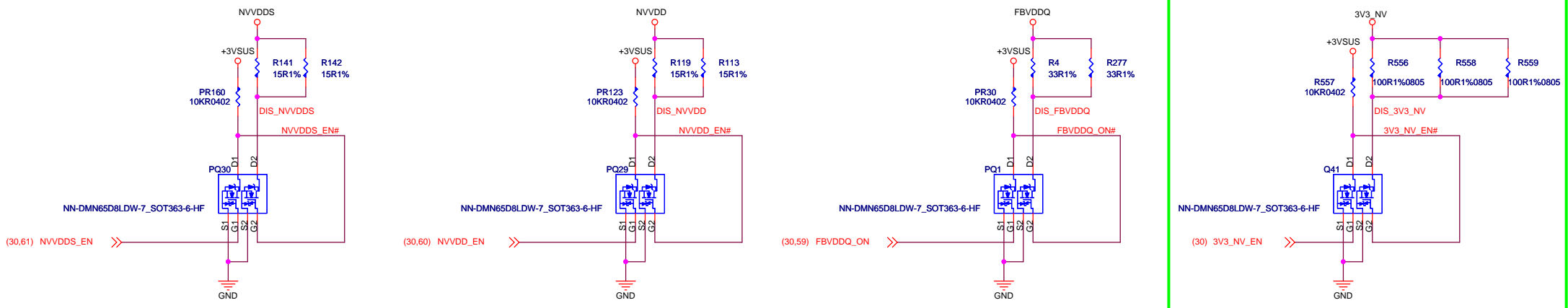


DGPU_Power Control



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Discharge



PEX_VDD 内部放电4ms

3V3_AON内部放电 2ms

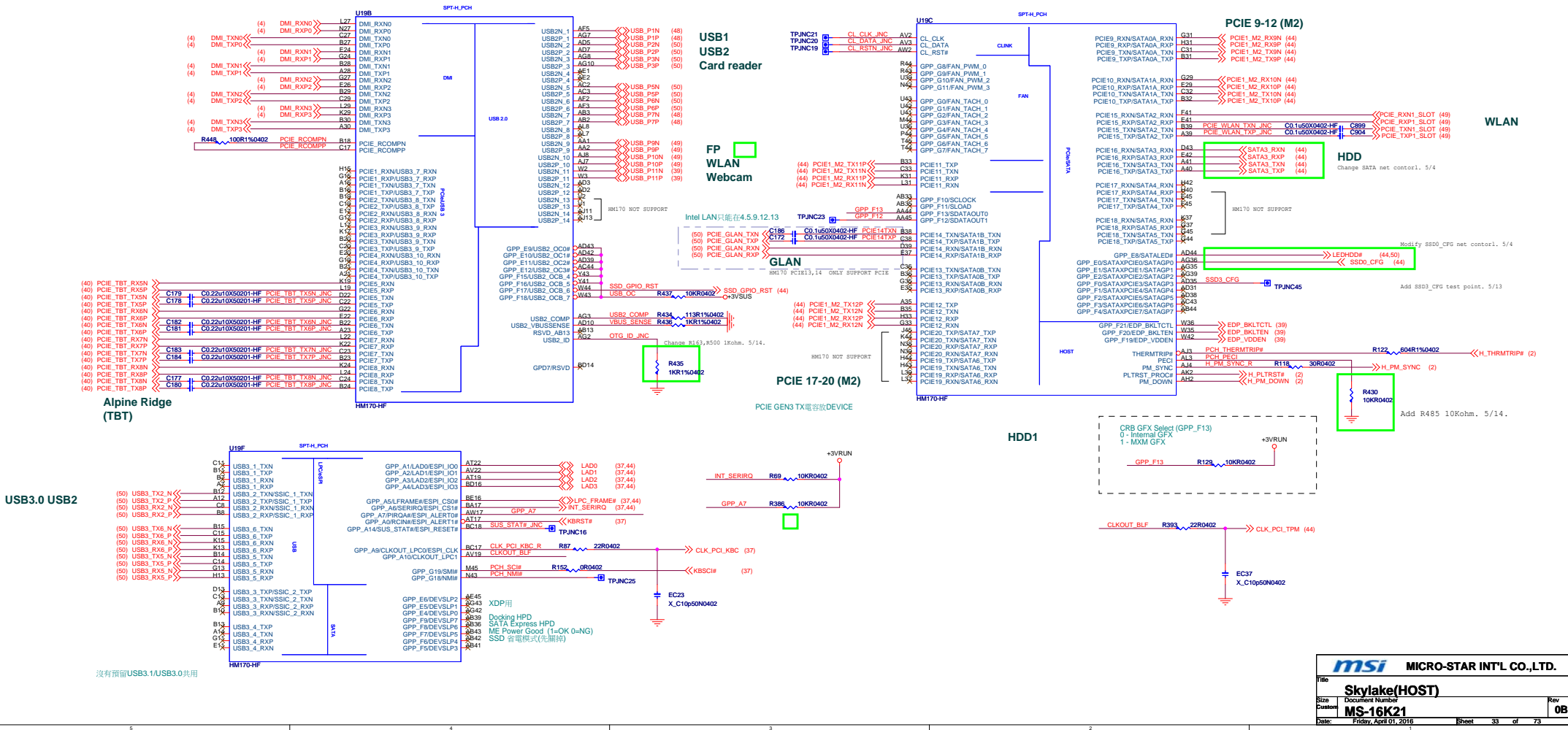
1V8AON内部放电2ms

1V8_MAIN内部放电320us

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Title DGPU Discharge	
Size A3	Document Number MS-16K21
Date: Wednesday, April 06, 2016	Sheet 31 of 73
Rev 0B	

USB3.0 USB2

沒有預留USB3.1/USB3.0共用



PCH EDS Page 52



S1	G1	S2	G2	検討漏電流
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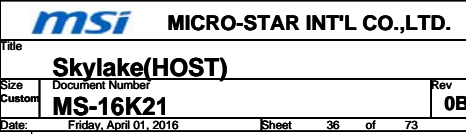
Skylake(HOST)

Size Custom	Document Number MS-16K21
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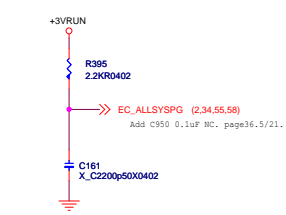
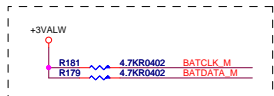
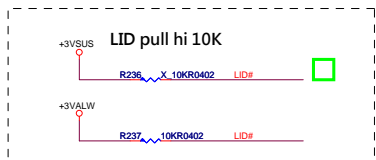
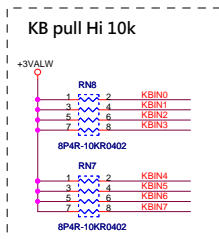
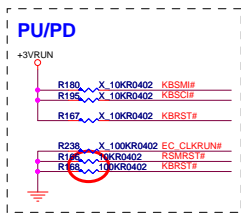
Date: Friday, April 08, 2016

Sheet 34 of 73

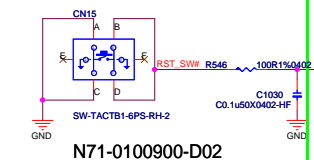
0E



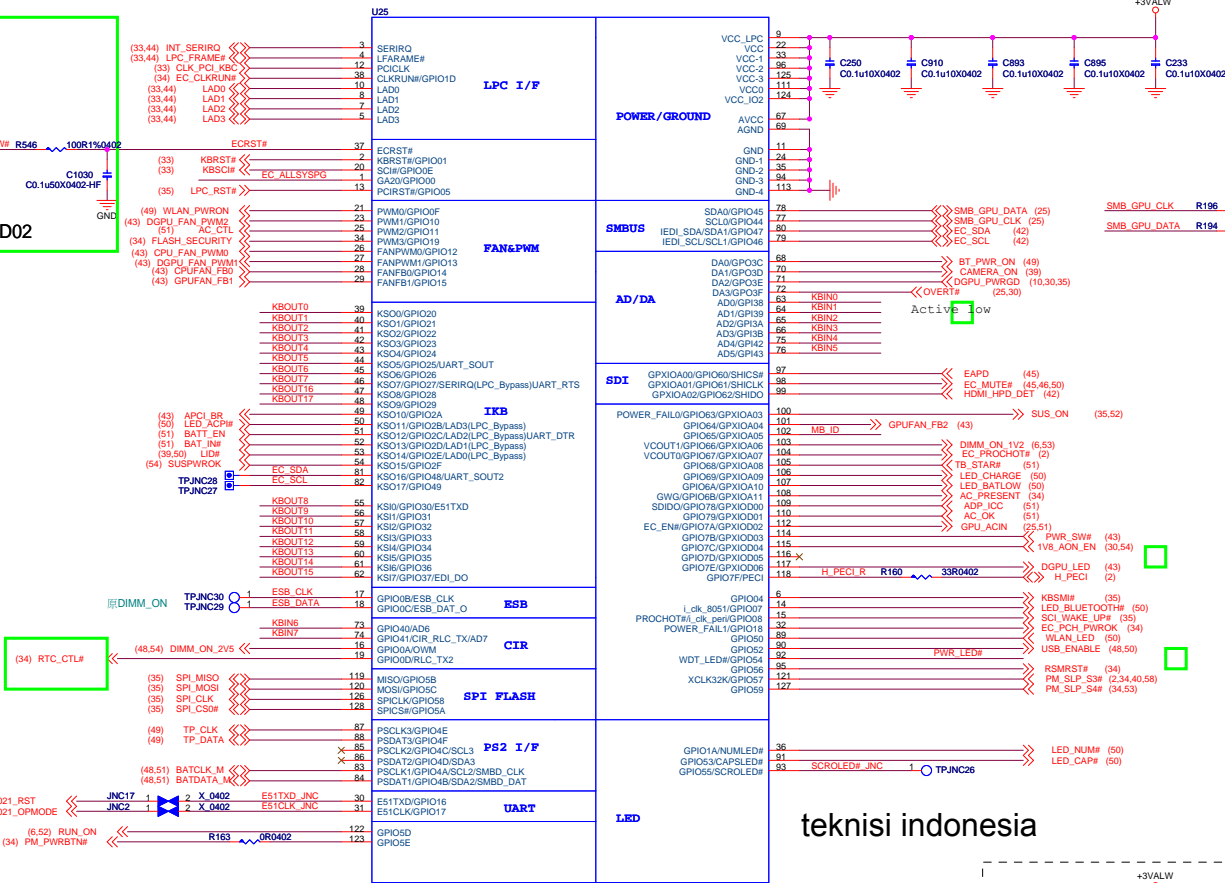
RSMRST# follow DG modify to 10K



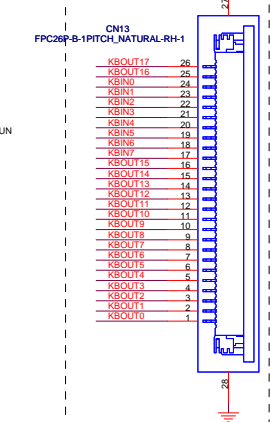
Hardware Reset



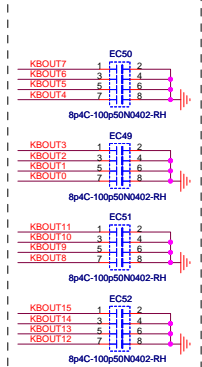
KBC/EC/uP (ENE9028)



N5A-26F0450-H06

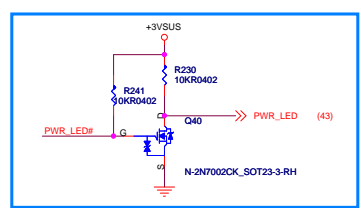


For EMI

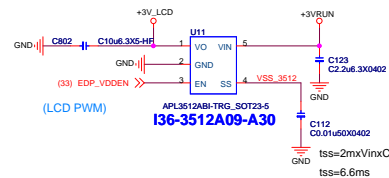


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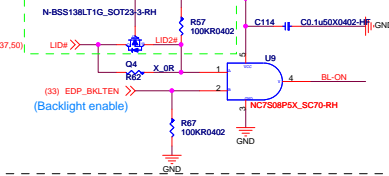
MotherBoard ID



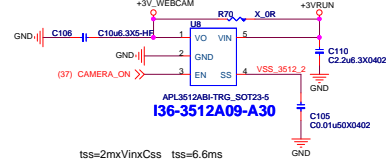
Pannel Device Logic Power



Backlight

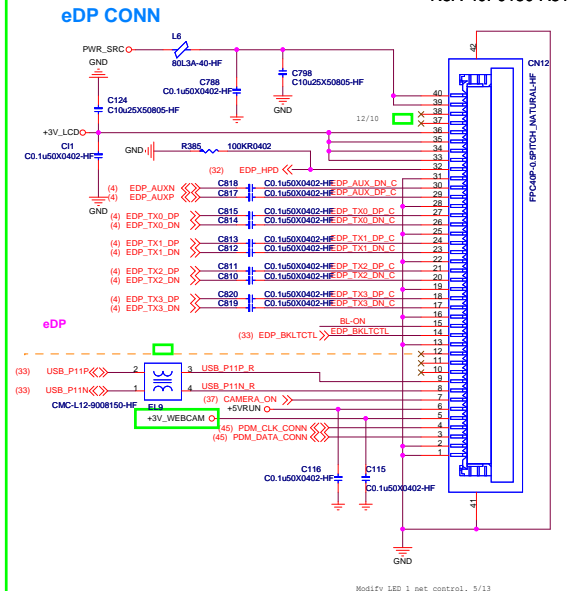


CAMERA Power



eDP Connector

N5A-40F0180-A81



LCD Module Pin Define FOR FULL HD PANEL

Pin No	Symbol	Description
1	Vcom SDA	Vcom IIC SDA
2	H_GND	High Speed Ground
3	LAN1_N	Complement Signal-Lane 1
4	LAN1_P	True Signal-Main Lane 1
5	H_GND	High Speed Ground
6	LAN0_N	Complement Signal-Lane 0
7	LAN0_P	True Signal-Main Lane 0
8	H_GND	High Speed Ground
9	AUX+	True Signal-Auxiliary Channel
10	AUX-	Complement Signal-Auxiliary Channel
11	H_GND	High Speed Ground
12	LCD_VCC	Power Supply +3.3 V (typical)
13	LCD_VCC	Power Supply +3.3 V (typical)
14	NC	No Connection (Reserved for CMI test)
15	H_GND	Ground
16	H_GND	Ground
17	HPD	Hot Plug Detect
18	BL_GND	BL Ground
19	BL_GND	BL Ground
20	BL_GND	BL Ground
21	BL_GND	BL Ground
22	BL_EN	BL_Enable Signal of LED Converter
23	BL_PWM	PWM Dimming Control Signal of LED Converter
24	Vcom SCL	Vcom IIC SCL
25	NC	No Connection (Reserved)
26	LED_VCCS	BL Power
27	LED_VCCS	BL Power
28	LED_VCCS	BL Power
29	LED_VCCS	BL Power
30	NC	No Connection (Reserved)

LCD Module Pin Define FOR WQHD PANEL

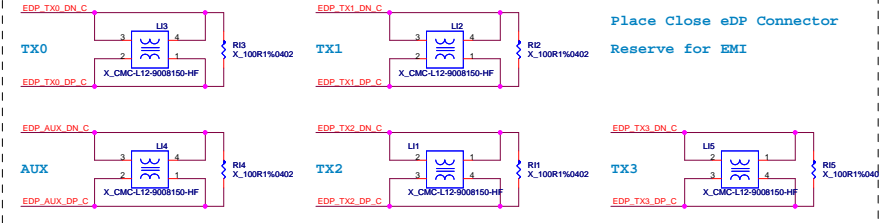
Pin No	Symbol	Description
1	NC	Reserved for LCD manufacturer's use
2	H_GND	High Speed Ground
3	Lane3_N	Complement Signal Link Lane 3
4	Lane3_P	True Signal Link Lane 3
5	H_GND	High Speed Ground
6	Lane2_N	Complement Signal Link Lane 2
7	Lane2_P	True Signal Link Lane 2
8	H_GND	High Speed Ground
9	Lane1_N	Complement Signal Link Lane 1
10	Lane1_P	True Signal Link Lane 1
11	H_GND	High Speed Ground
12	Lane0_N	Complement Signal Link Lane 0
13	Lane0_P	True Signal Link Lane 0
14	H_GND	High Speed Ground
15	AUX_CH_P	True Signal Auxiliary Channel
16	AUX_CH_N	Complement Signal Auxiliary Channel
17	H_GND	High Speed Ground
18	VDD	LCD logic and driver power(3.3V)
19	VDD	LCD logic and driver power(3.3V)
20	VDD	LCD logic and driver power(3.3V)
21	VDD	LCD logic and driver power(3.3V)
22	BIST	BIST patterns selection L : Disable [default] , H : Enable
23	LCD_GND	LCD logic and driver ground
24	LCD_GND	LCD logic and driver ground
25	LCD_GND	LCD logic and driver ground
26	LCD_GND	LCD logic and driver ground
27	HPD	HPD signal pin
28	BL_GND	Backlight ground
29	BL_GND	Backlight ground
30	BL_GND	Backlight ground
31	BL_GND	Backlight ground
32	BL_ENABLE	Backlight On/Off
33	BL_PWM_DIM	System PWM
34	NC	Reserved for LCD manufacturer's use
35	NC	Reserved for LCD manufacturer's use
36	VBL	Backlight power
37	VBL	Backlight power
38	VBL	Backlight power
39	VBL	Backlight power
40	NC	No Connection (Reserved)

LCD Module Pin Define FOR QHD+ PANEL

Pin No	Symbol	Description
1	NC	Reserved for LCD manufacturer's use
2	H_GND	High Speed Ground
3	Lane3_N	Complement Signal Link Lane 3
4	Lane3_P	True Signal Link Lane 3
5	H_GND	High Speed Ground
6	Lane2_N	Complement Signal Link Lane 2
7	Lane2_P	True Signal Link Lane 2
8	H_GND	High Speed Ground
9	Lane1_N	Complement Signal Link Lane 1
10	Lane1_P	True Signal Link Lane 1
11	H_GND	High Speed Ground
12	Lane0_N	Complement Signal Link Lane 0
13	Lane0_P	True Signal Link Lane 0
14	H_GND	High Speed Ground
15	AUX_CH_P	True Signal Auxiliary Channel
16	AUX_CH_N	Complement Signal Auxiliary Channel
17	H_GND	High Speed Ground
18	NC	Reserved for LCD manufacturer's use
19	NC	Reserved for LCD manufacturer's use
20	VDD	LCD logic and driver power(3.3V)
21	VDD	LCD logic and driver power(3.3V)
22	VDD	LCD logic and driver power(3.3V)
23	VDD	LCD logic and driver power(3.3V)
24	VDD	LCD logic and driver power(3.3V)
25	NC	Reserved for LCD manufacturer's use
26	LCD_GND	LCD logic and driver ground
27	LCD_GND	LCD logic and driver ground
28	LCD_GND	LCD logic and driver ground
29	LCD_GND	LCD logic and driver ground
30	LCD_GND	LCD logic and driver ground
31	HPD	HPD signal pin
32	NC	Reserved for LCD manufacturer's use
33	PWM_OUT	PWM_OUT
34	PWM_IN	PWM_IN
35	NC	Reserved for LCD manufacturer's use
36	NC	Reserved for LCD manufacturer's use
37	NC	Reserved for LCD manufacturer's use
38	VBL	LED Anode
39	VBL	LED Anode
40	NC	Reserved for LCD manufacturer's use
41	LED_C1	LED Cathode 1
42	LED_C2	LED Cathode 2
43	LED_C3	LED Cathode 3
44	LED_C4	LED Cathode 4
45	LED_C5	LED Cathode 5
46	LED_C6	LED Cathode 6
47	LED_C7	LED Cathode 7
48	LED_C8	LED Cathode 8
49	NC	Reserved for LCD manufacturer's use
50	NC	Reserved for LCD manufacturer's use

Place Close eDP Connector

Reserve for EMI



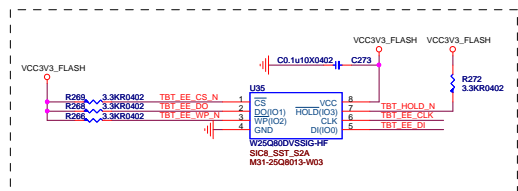
Thunderbolt

DDI C
HDMI

DDI B
DP

CIO1
CIO0

B07-L634005-I06



VCC3V3_FLASH VCC3V3_FLASH

CPUDPC_SCL R488 X 2.2K R0402

CPUDPC_SDA R489 X 2.2K R0402

TBT_LSTX R270 1M R0402

TBT_LSRX R271 1M R0402

TBT_FORCE_PWR R496 100K R0402

TBT_SRC_CPGI R204 100K R0402

TBT_LC_SCL R229 3.3K R0402

TBT_LC_SDA R230 3.3K R0402

TBT_PCH_WAKE_N R251 10K R0402

TBT_CIO_PLUG_EVENT_N R252 10K R0402

TBT_BATLOW_N R253 10K R0402

TBT_DC_INT R254 10K R0402

TBT_FORCE_PWR R255 10K R0402

TBT_CIO_PWR_EN R256 10K R0402

TBT_CIO_PWR_EN R257 10K R0402

TBT_SRC_CPGI R258 10K R0402

TBT_SRC_CPGI R259 10K R0402

TBT_SRC_CPGI R260 10K R0402

TBT_SRC_CPGI R261 10K R0402

TBT_SRC_CPGI R262 10K R0402

TBT_SRC_CPGI R263 10K R0402

TBT_SRC_CPGI R264 10K R0402

TBT_SRC_CPGI R265 10K R0402

TBT_SRC_CPGI R266 10K R0402

TBT_SRC_CPGI R267 10K R0402

TBT_SRC_CPGI R268 10K R0402

Reserve for HDMI compliance test rise/fall time fail.
The accurate value is 1pf 6.3V 0201 cap.

2015/08/17 Add

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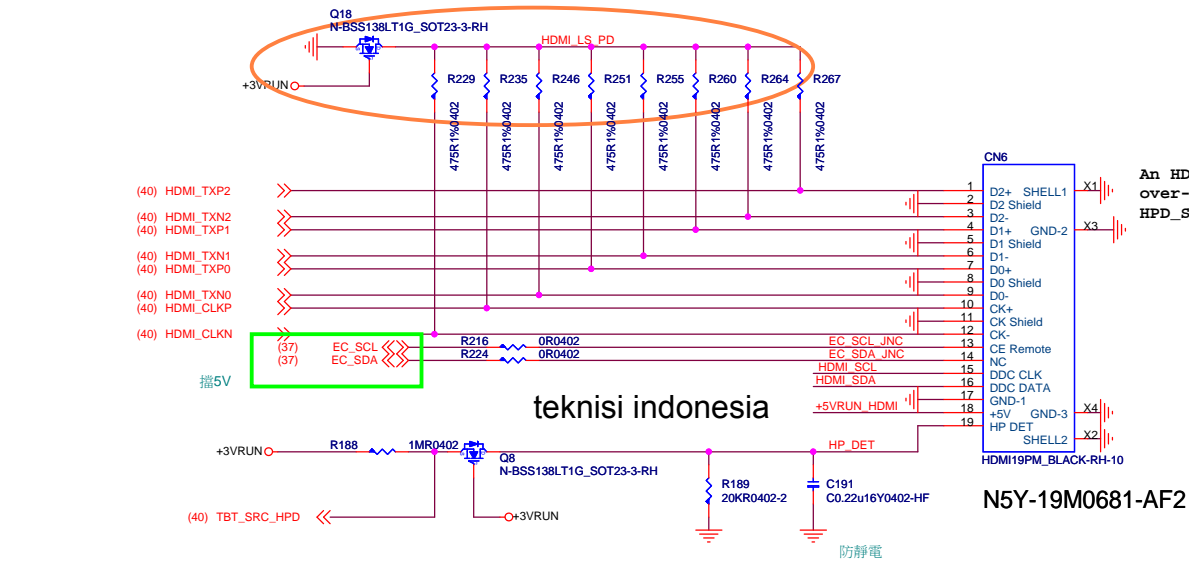
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Alpine Ridge(TBT)

MS-16K21

Friday, April 01, 2016 Sheet 40 of 73

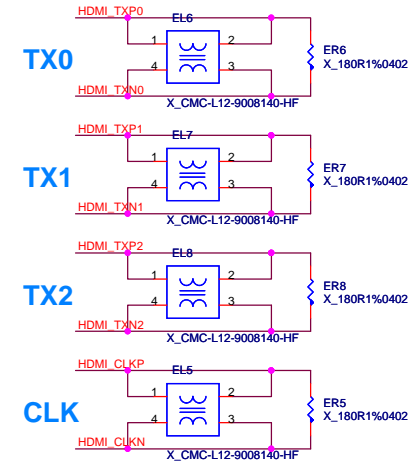
HDMI connector



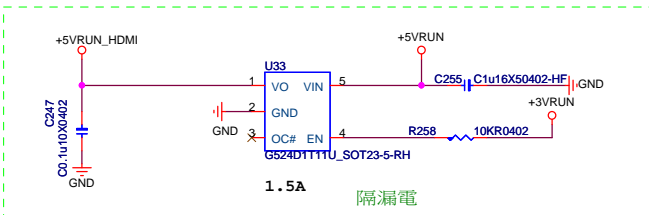
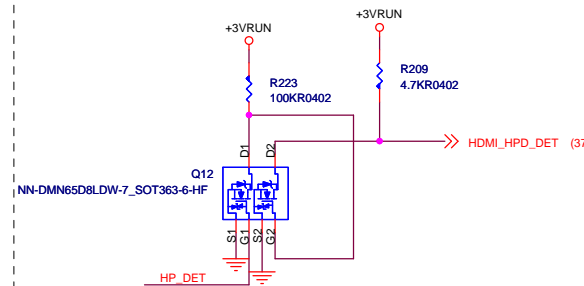
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N5Y-19M0681-AF2

EMI Close Connector

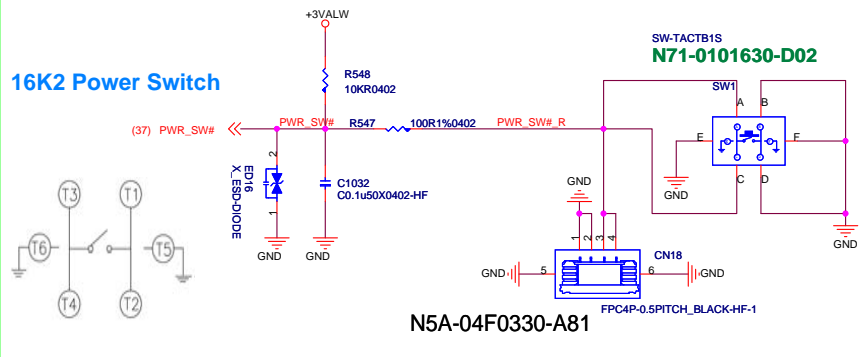


HPD Level Shift 5V to 3V



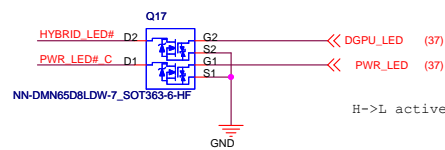
PWR SW/CPU FAN/BTB CONN/ LED CONN

16K2 Power Switch



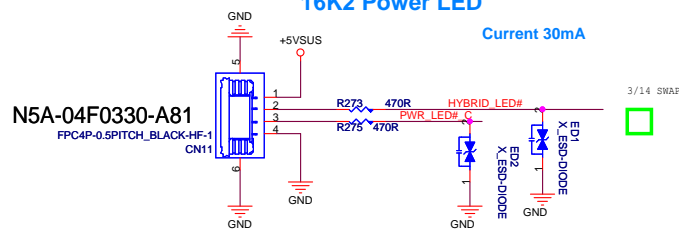
Control PWR LED

DGPU_LED	PWR_LED	LED COLOR
L	H	RED
H	H	ORANGE
H	L	GREEN
L	L	X



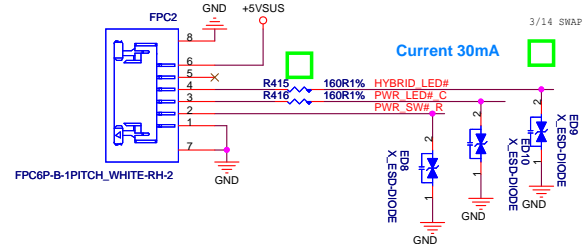
16K2 Power LED

Current 30mA

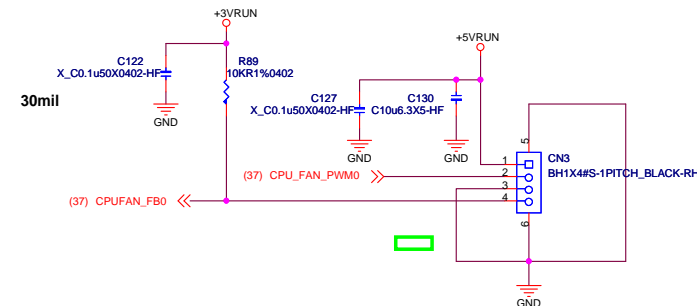


Power LED+SW for 17B1

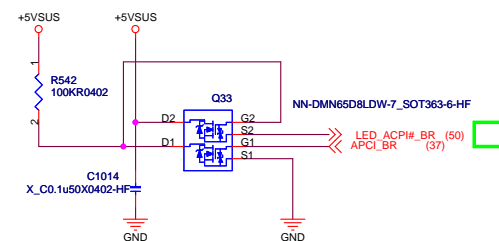
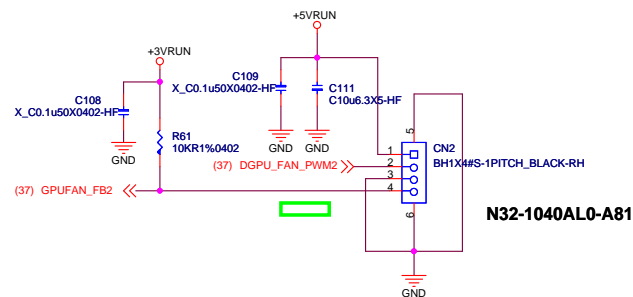
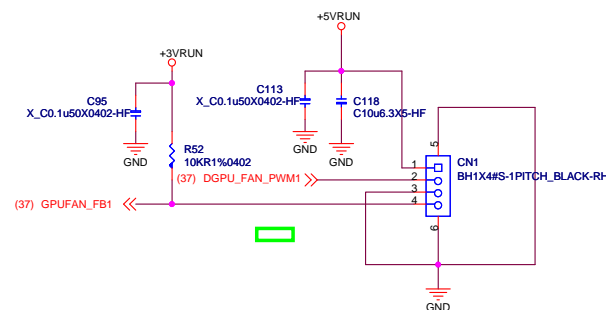
Current 30mA



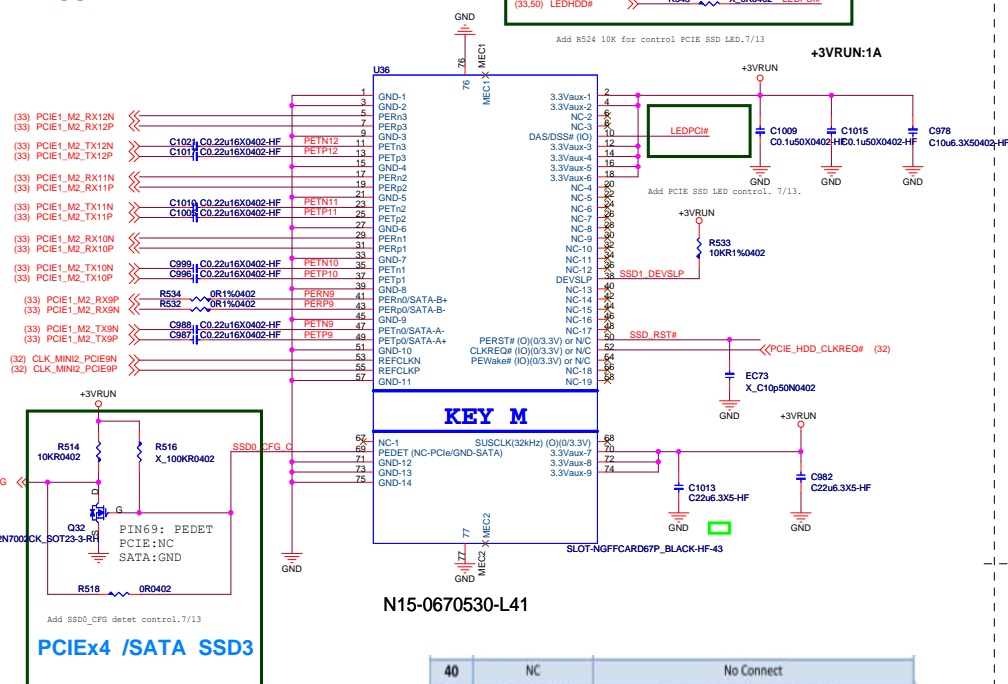
CPU FAN



DGPU FAN

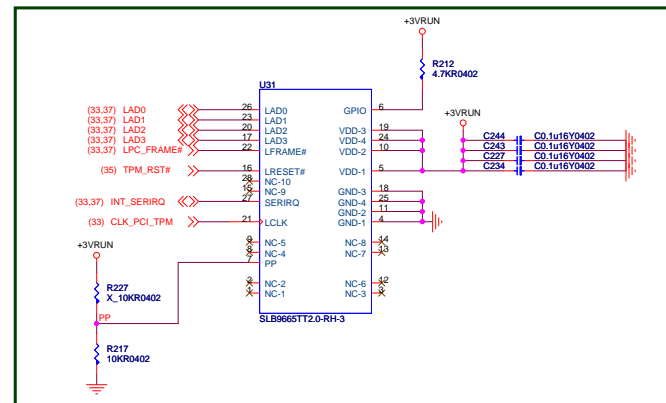


M2 SSD



N15-0670530-L41

TPM



Physical Presence (PP)
The standard position of the jumper should connect the pin to GND. If the pin is connected to VDD, some special commands are enabled.

DE1/DE2	CH1/CH2De-Emphasis dB (at 6Gbps)	EQ1/EQ2	CH1/CH2Equalization dB (at 6Gbps)
NC (default)	-4	NC (default)	0
0	0	0	7
1	-2	1	14

DEW1/DEW2	Device Function → DE Width for CH1/CH2
0	De-emphasis pulse duration, short (recommended setting when link operates at SATA 1.5/3/6 Gbps)
1 (default)	De-emphasis pulse duration, long (recommended setting when link operates at SATA 1.5/3 Gbps speed only)



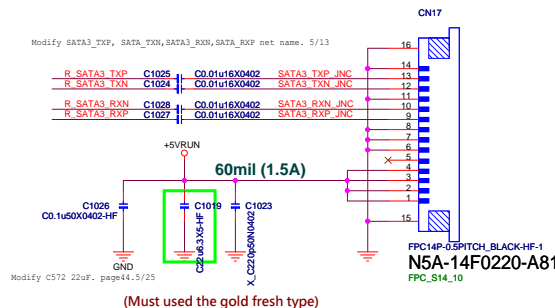
TI SN75LVCP601RTJR HW Setting

HDD2

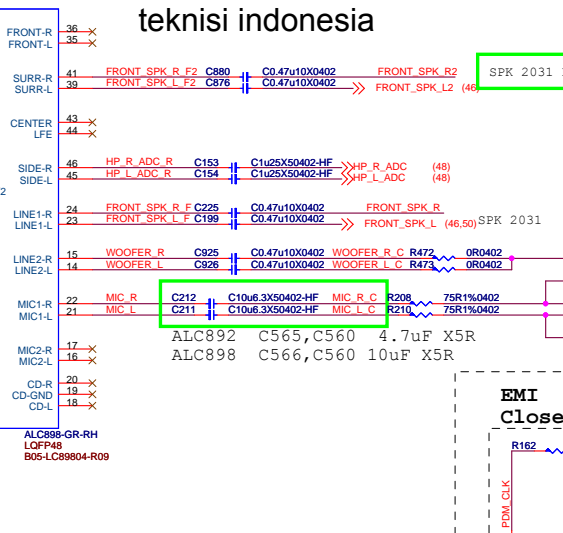
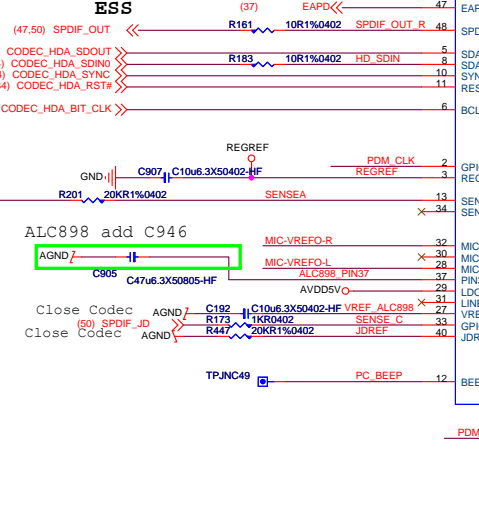
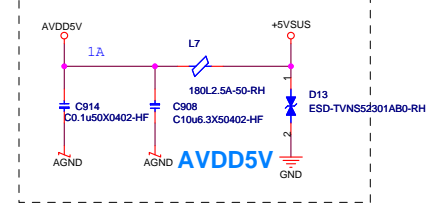
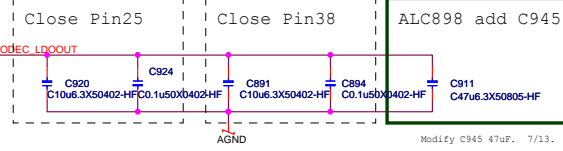
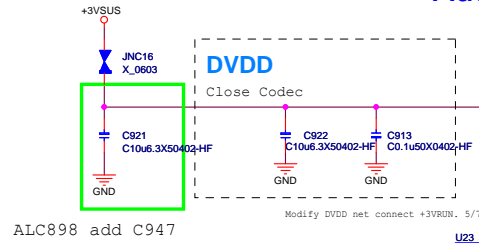
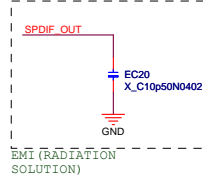
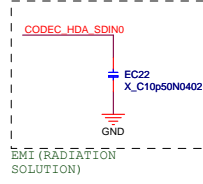
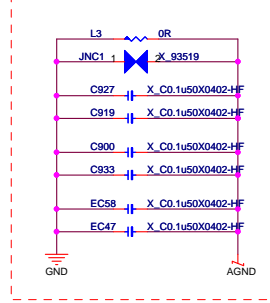
HDD (With Repeater)

I98-756010C-T07

HDD GEN3 Repeater



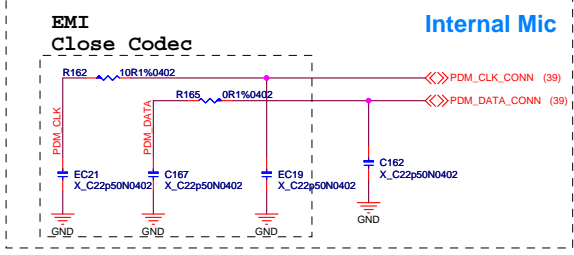
Audio CODEC/Audio AMP



SPK 2031 FOR 17B1

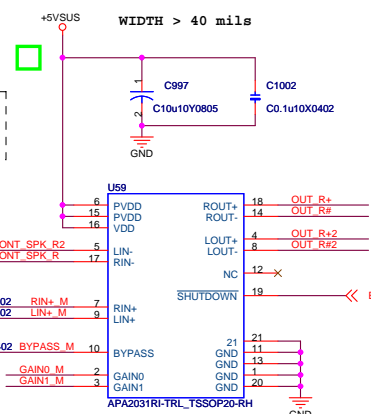
FOR 17B1

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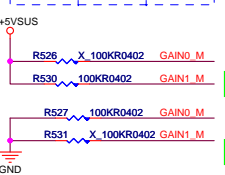


10dB / 2W

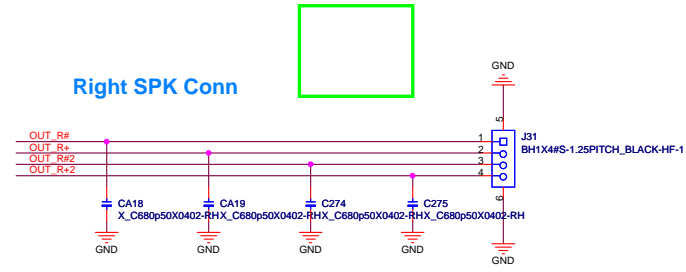
6 dB / 1.7 W
2W Speaker



Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X



Right SPK Conn



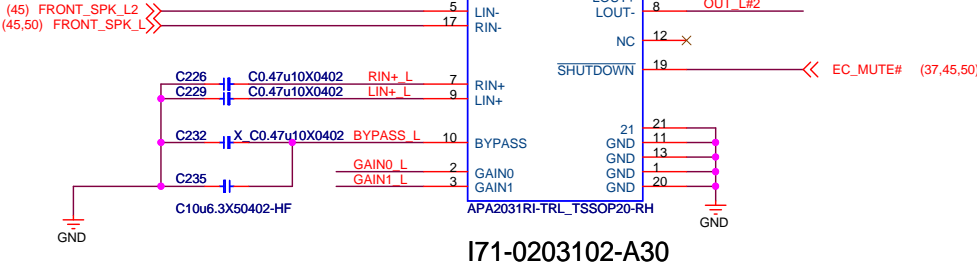
I71-0203102-A30

SPK LEFT /Woffer FOR 17B1

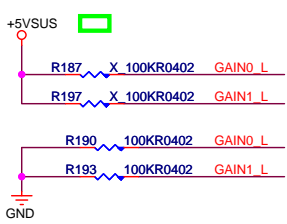
10DB / 2W

WIDTH > 40 mils

6 dB / 1.7 W
2W Speaker



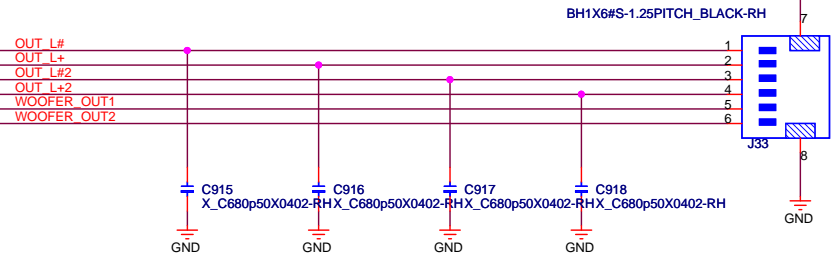
I71-0203102-A30



For APA2031

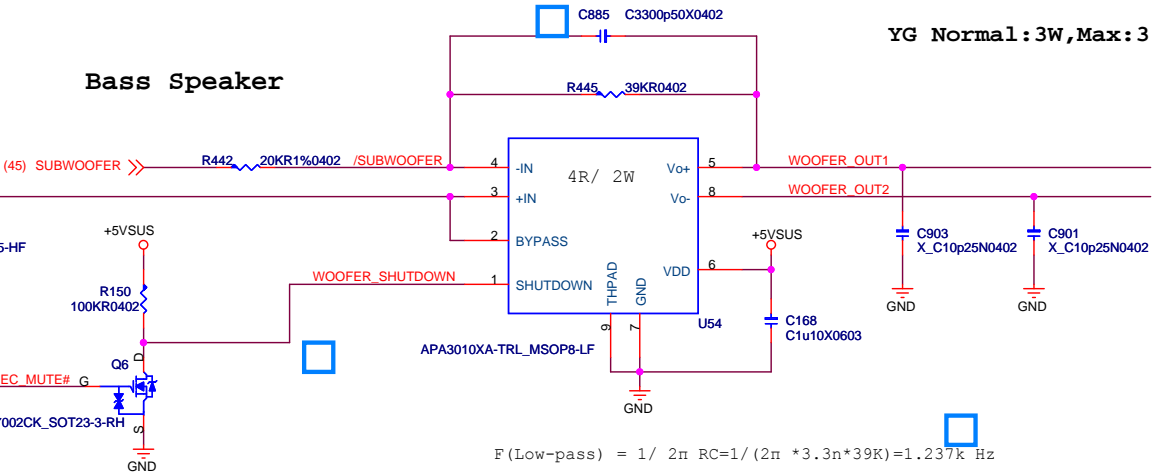
Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X

Conn



Bass Speaker

YG Normal:3W,Max:3.5W 4ohm



$$F(\text{Low-pass}) = 1 / 2\pi RC = 1 / (2\pi * 3.3n * 39K) = 1.237k \text{ Hz}$$

MICRO-STAR INT'L CO.,LTD.

Title

SPK LEFT/WOOFER

Size B

Document Number

MS-16K21

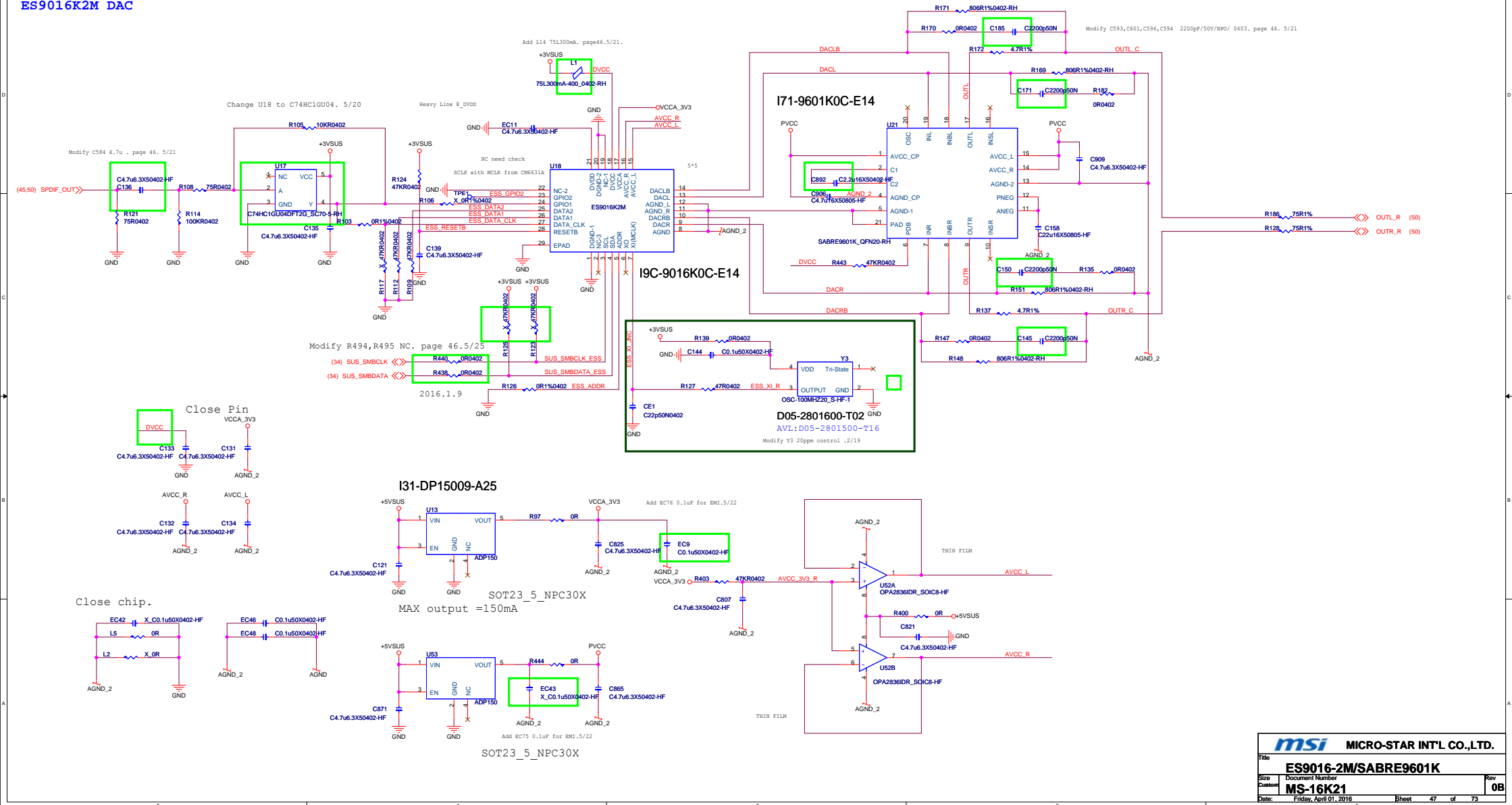
Date: Friday, April 01, 2016

Sheet 46 of 73

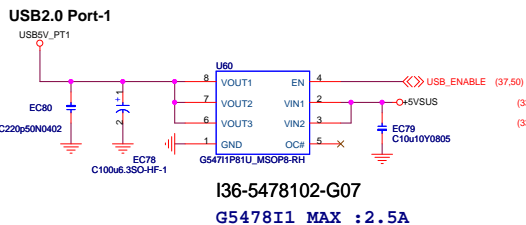
Rev

0B

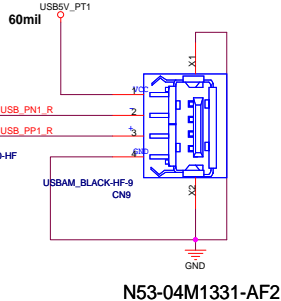
ES9016K2M DAC



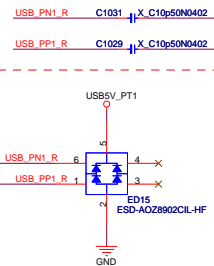
USB2.0 CNT-1



USB2.0/Keyboard control



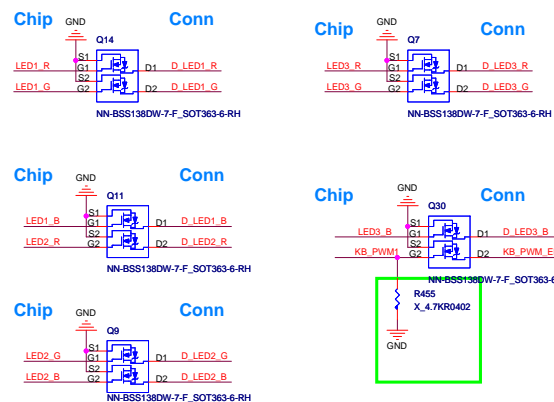
EMI



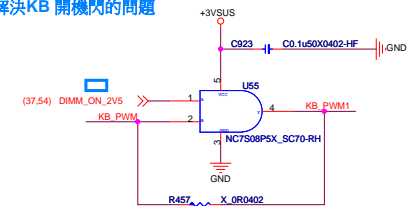
www.teknisi-indonesia.com

LED 8051 Controller

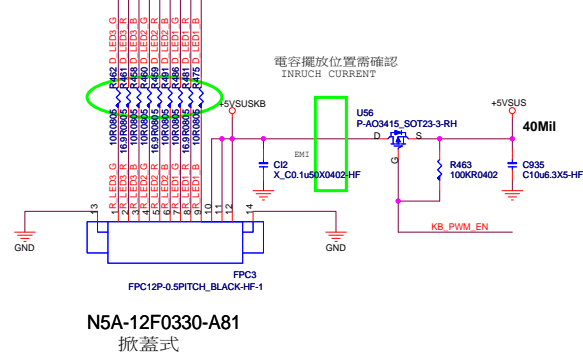
EPF021J Sink current not enough, only using BSS138 (0.22A)



解決KB 開機閃的問題



LED Keyboard CONN



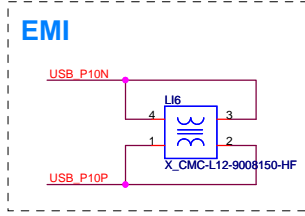
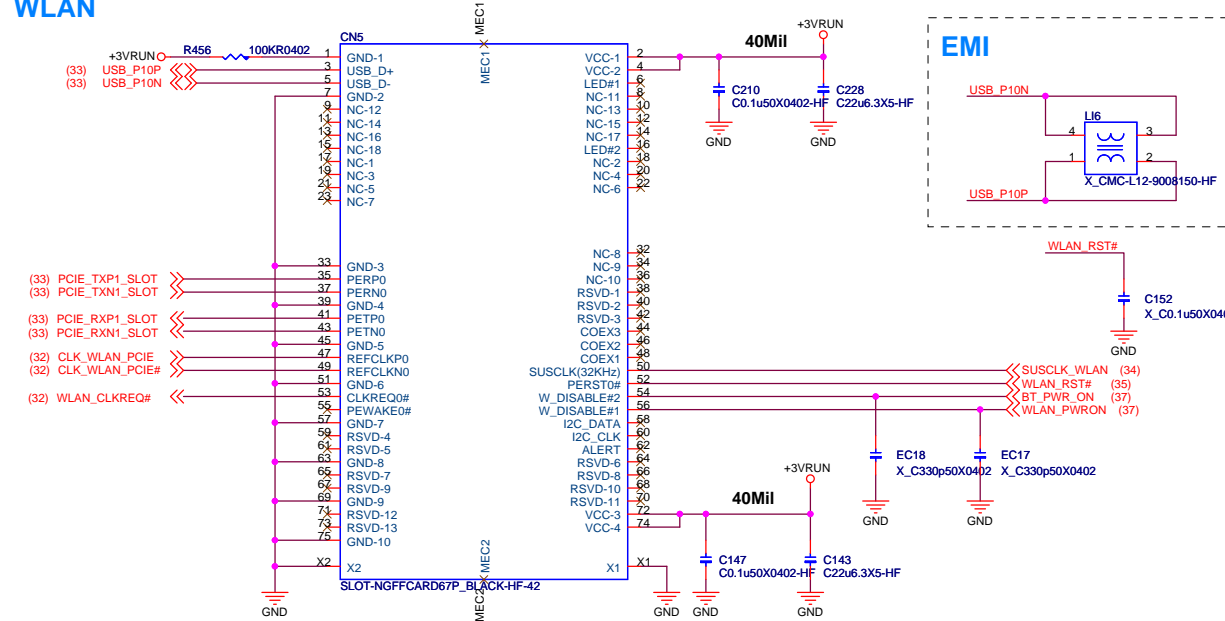
LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

msi MICRO-STAR INT'L CO.,LTD.

File
USB 3.0 connector
Size
P
Document Number
MS-16K21
Date
Wednesday, April 06, 2016
Sheet
48
of
73
Rev
0B

WLAN /ClickPad/FP

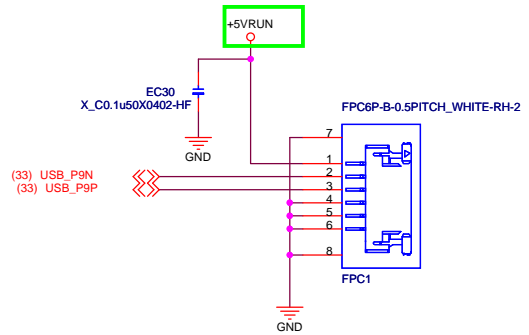
WLAN



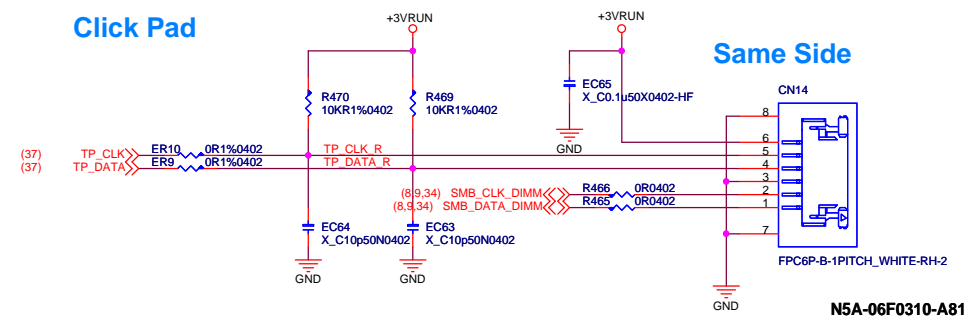
Pin 1	GND	Pin 2	3.3V
Pin 3	USB_D+	Pin 4	3.3V
Pin 5	USB_D-	Pin 6	LED1#
Pin 7	GND	Pin 8	Module Key
Pin 9	Module Key	Pin 10	Module Key
Pin 11	Module Key	Pin 12	Module Key
Pin 13	Module Key	Pin 14	Module Key
Pin 15	N/C	Pin 16	LED2#
Pin 17	N/C	Pin 18	GND
Pin 19	N/C	Pin 20	N/C
Pin 21	N/C	Pin 22	N/C
Pin 23	Module Key	Pin 24	Module Key
Pin 25	Module Key	Pin 26	Module Key
Pin 27	Module Key	Pin 28	Module Key
Pin 29	Module Key	Pin 30	Module Key
Pin 31	Module Key	Pin 32	N/C
Pin 33	GND	Pin 34	N/C
Pin 35	PERP0	Pin 36	N/C
Pin 37	PERN0	Pin 38	Clink Reset (I 3.3V)
Pin 39	GND	Pin 40	N/C
Pin 41	PETP0	Pin 42	N/C
Pin 43	PETN0	Pin 44	N/C
Pin 45	GND	Pin 46	N/C
Pin 47	REFCLKP0	Pin 48	N/C
Pin 49	REFCLKN0	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 51	GND	Pin 52	PERST0#
Pin 53	CLKREQ0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 55	PEWAKE0#	Pin 56	WLAN_EN (W_DISABLE2#)
Pin 57	N/C	Pin 58	N/C
Pin 59	N/C	Pin 60	N/C
Pin 61	N/C	Pin 62	N/C
Pin 63	GND	Pin 64	Resever
Pin 65	N/C	Pin 66	N/C
Pin 67	N/C	Pin 68	N/C
Pin 69	GND	Pin 70	N/C
Pin 71	N/C	Pin 72	3.3V
Pin 73	N/C	Pin 74	3.3V
Pin 75	GND		

N15-0670520-L41
SLOT_NGFFCARD67_H2_15

Finger Print



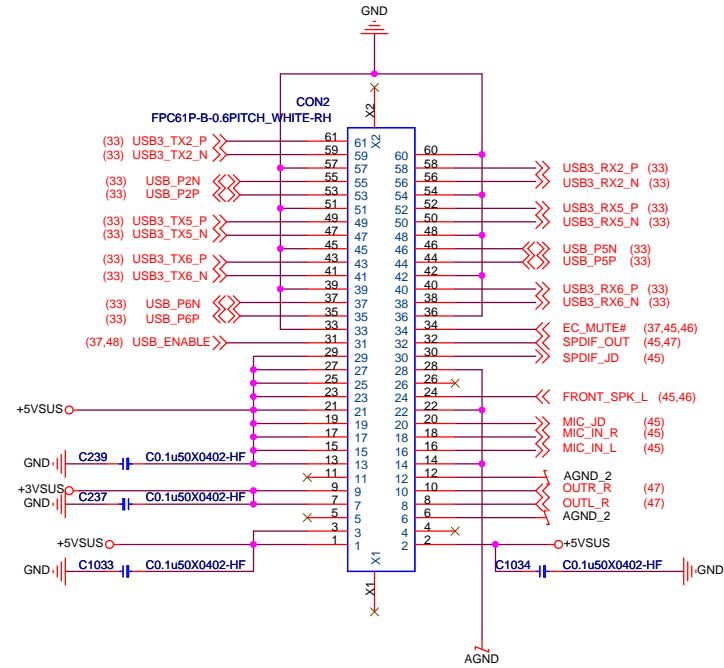
Click Pad



N5A-06F0310-A81

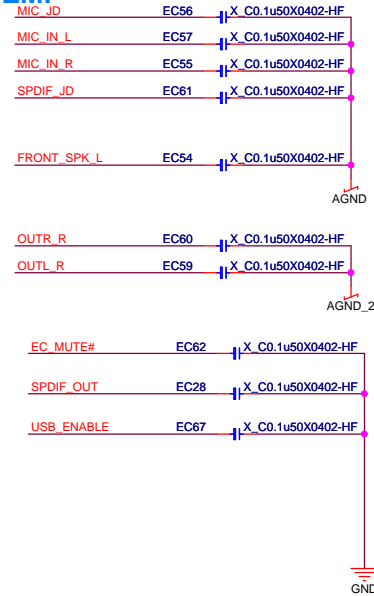
R473 , R479 0ohm on part for TP SMBus function. 7/15

(Audio CONN/USB3.0)

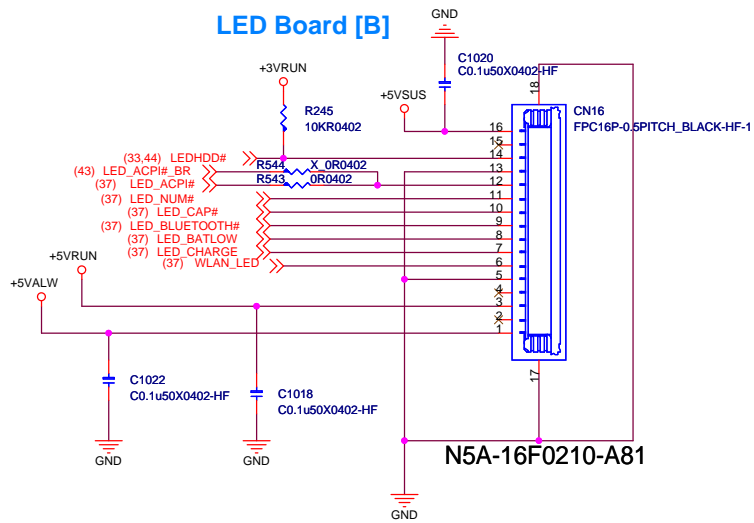


16K2 BTB CONN

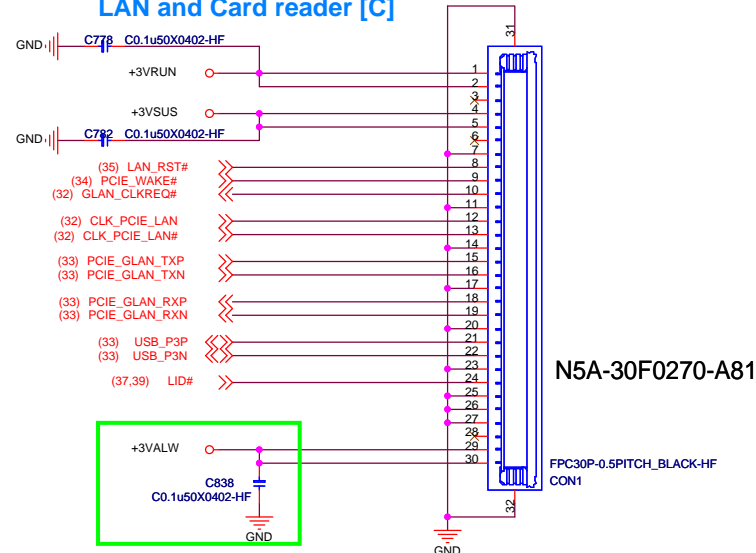
EMI



LED Board [B]



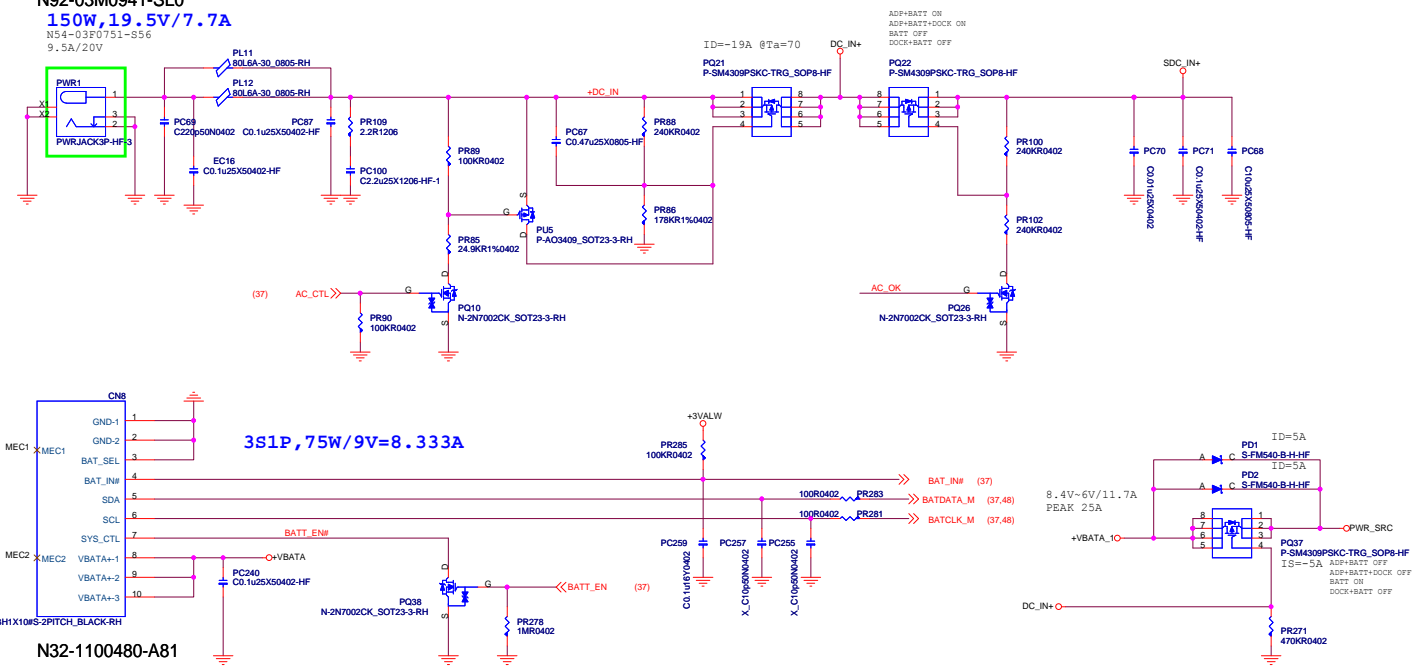
LAN and Card reader [C]



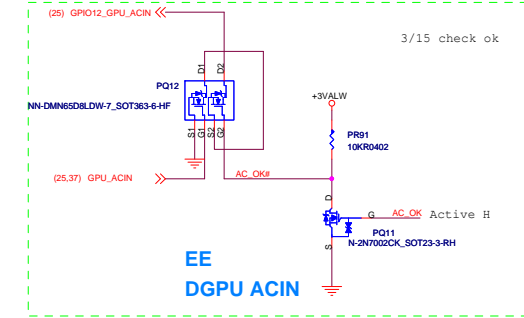
N5A-30F0270-A81

FPC30P-0.5PITCH_BLACK-HF
CON1

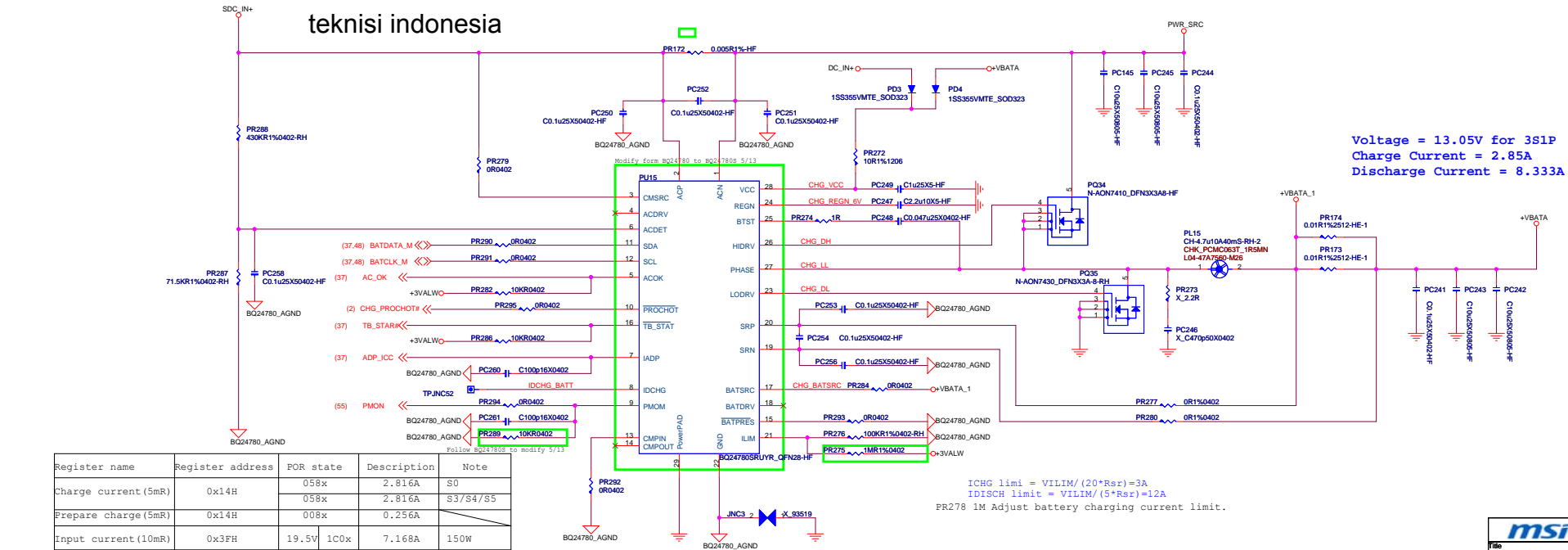
N92-03M0941-SLO
150W, 19.5V/7.7A
N54-0380751-S56
9.5A/20V



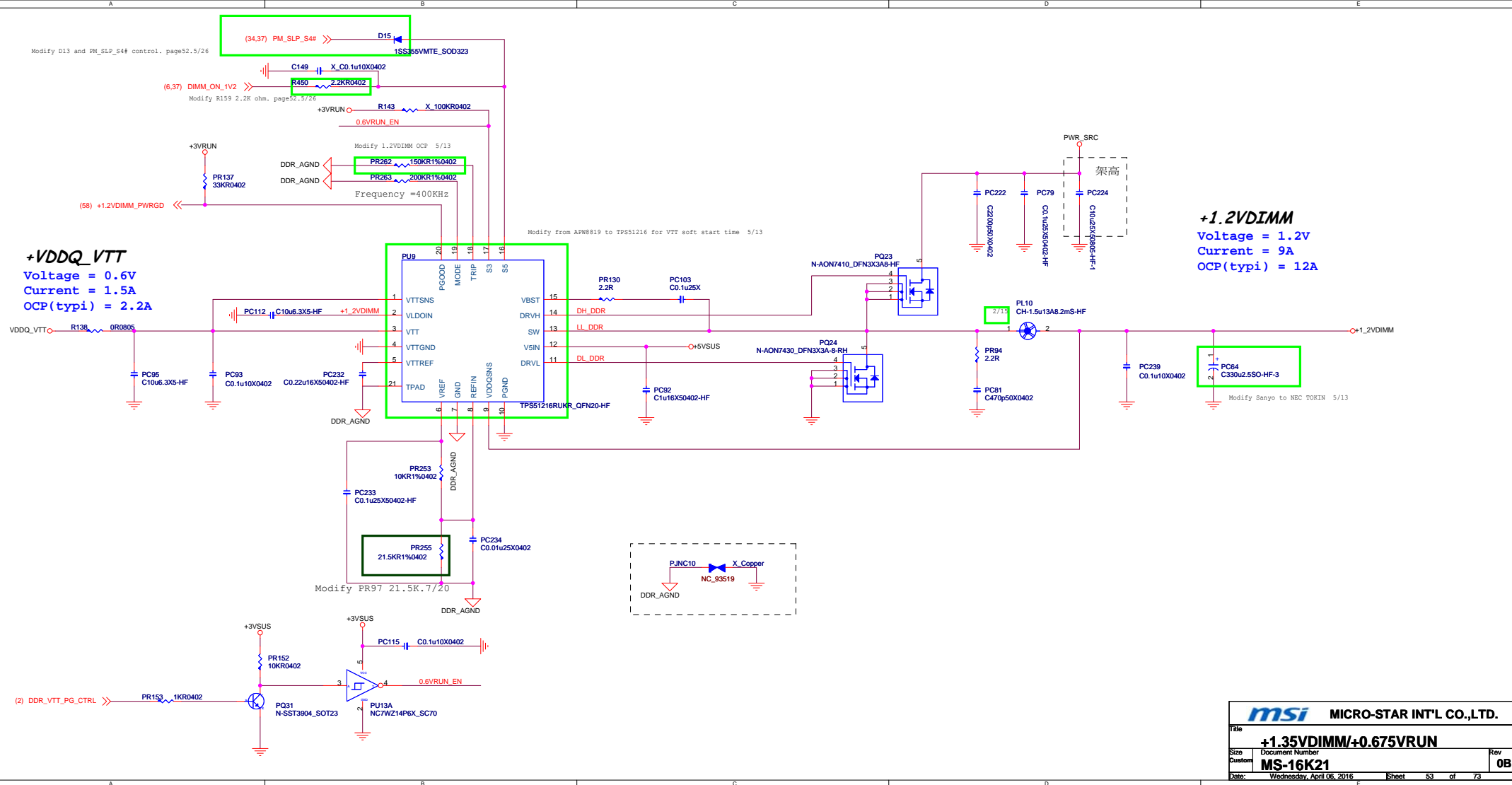
AC_OK#	GPU_ACIN (EC control)	GPIO12_GPU_ACIN
0	0	AC
0	1	AC
1	0	AC
1	1	DC

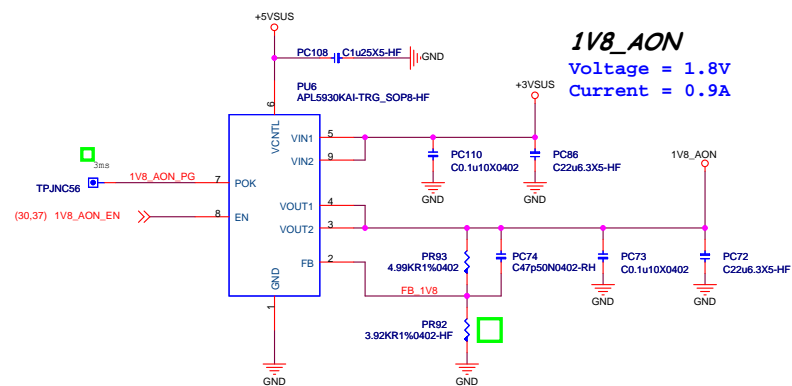
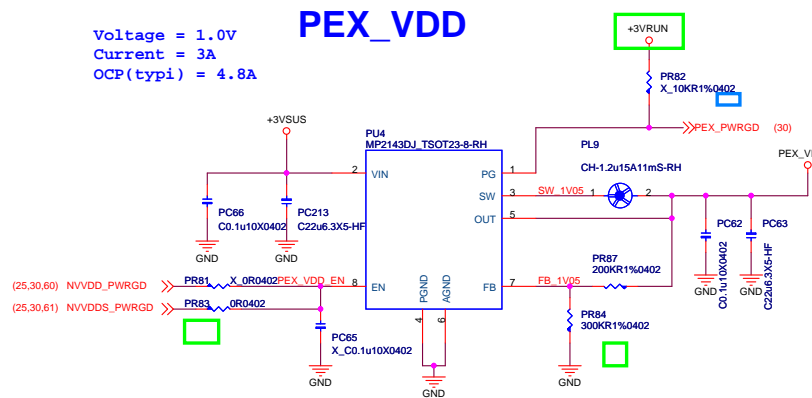
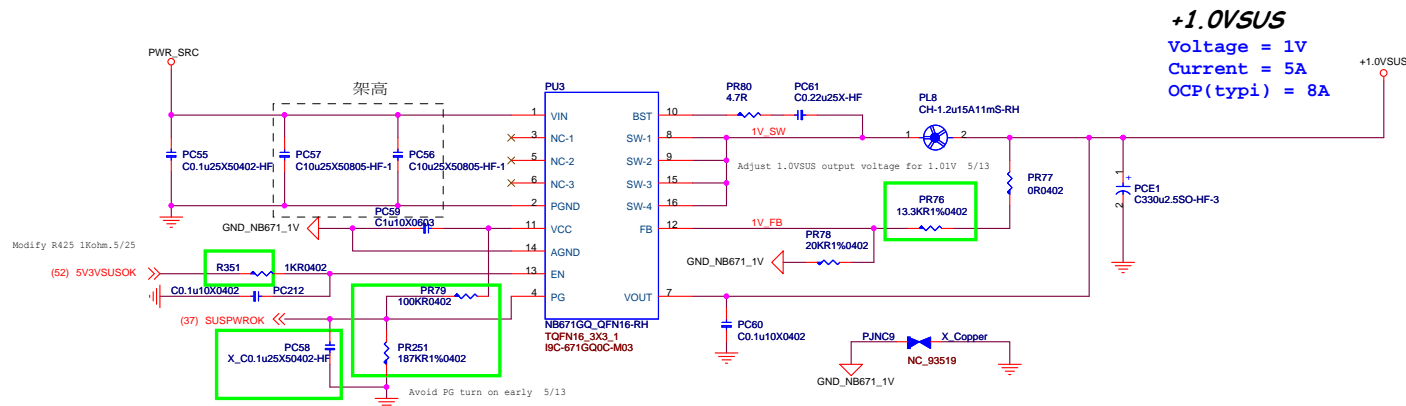
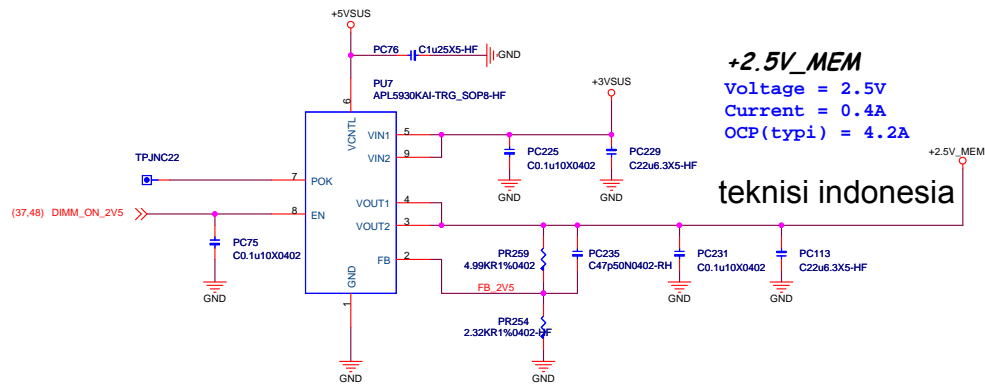


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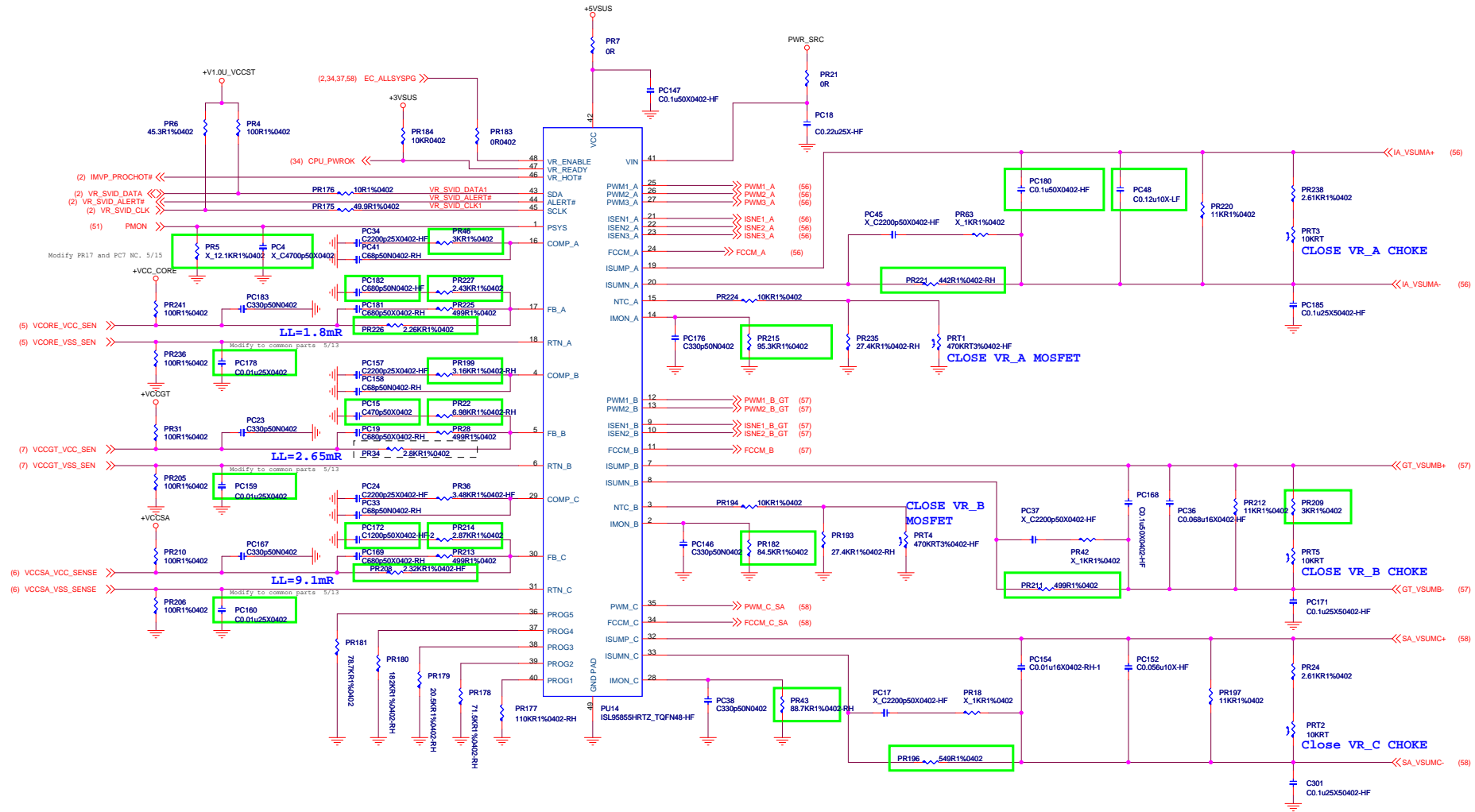
Register name	Register address	POR state	Description	Note
Charge current (5mR)	0x14H	058x	2.816A	S0
Prepare charge (5mR)	0x14H	058x	2.816A	S3/S4/S5
Input current (10mR)	0x3FH	19.5V 1C0x	7.168A	150W
Charge voltage	0x15H	330x	13.056V	3S1P
Discharge current (5mR)	0x39H	06xx	3.072A	BOOST current





Skylake H-line 42 45W ISL95855

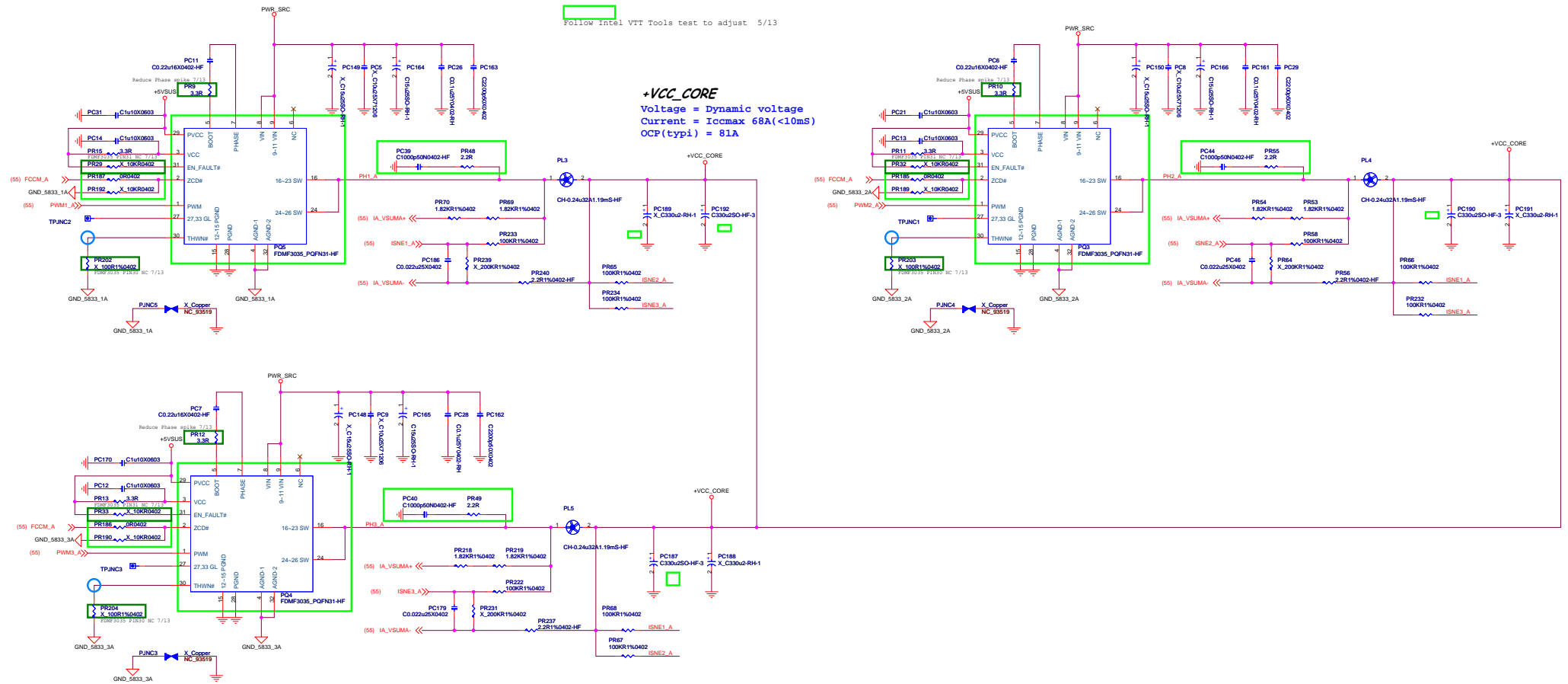
Follow Intel VTT Tools test result to adjust 5/13

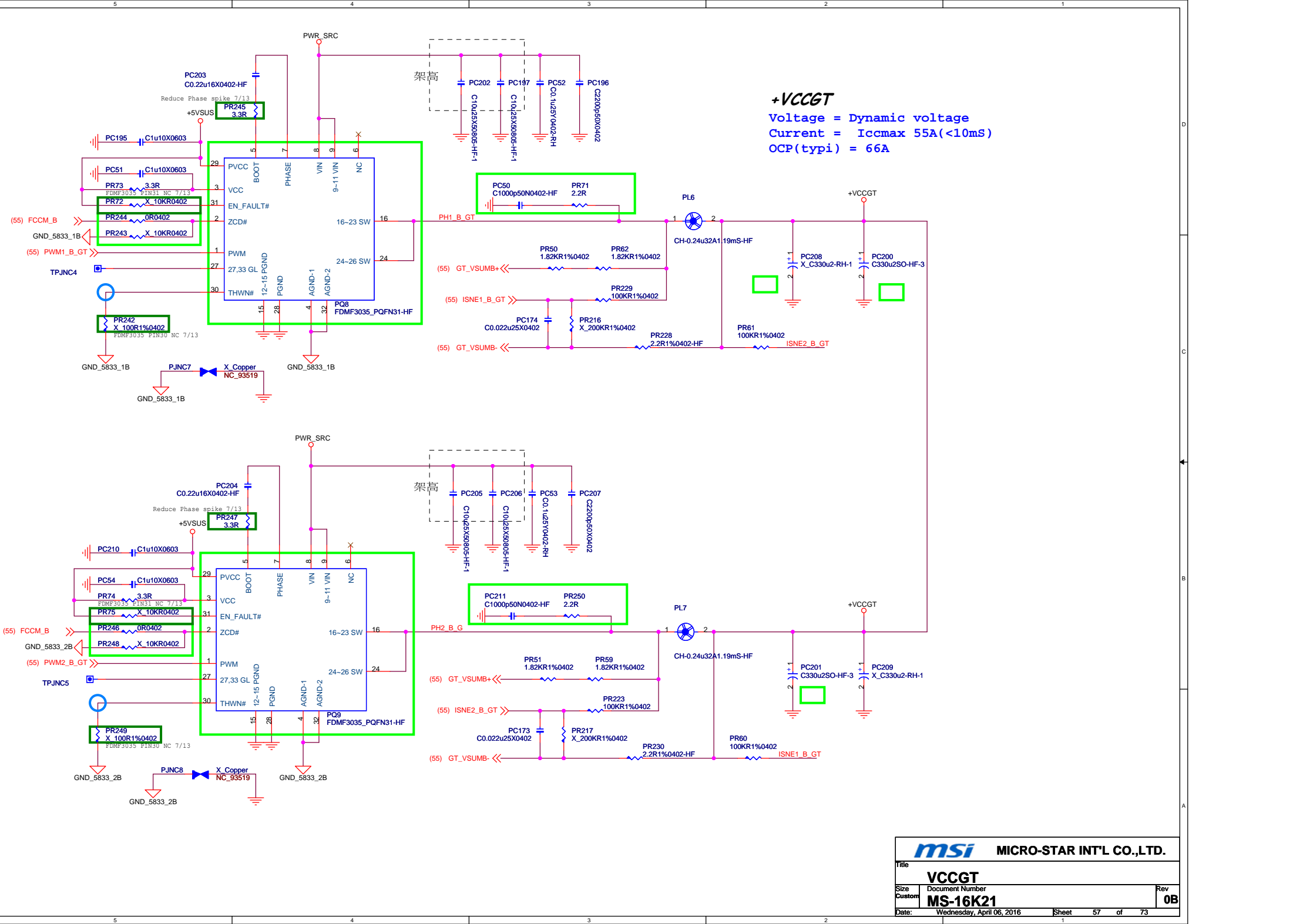


SKL-H (4+2)

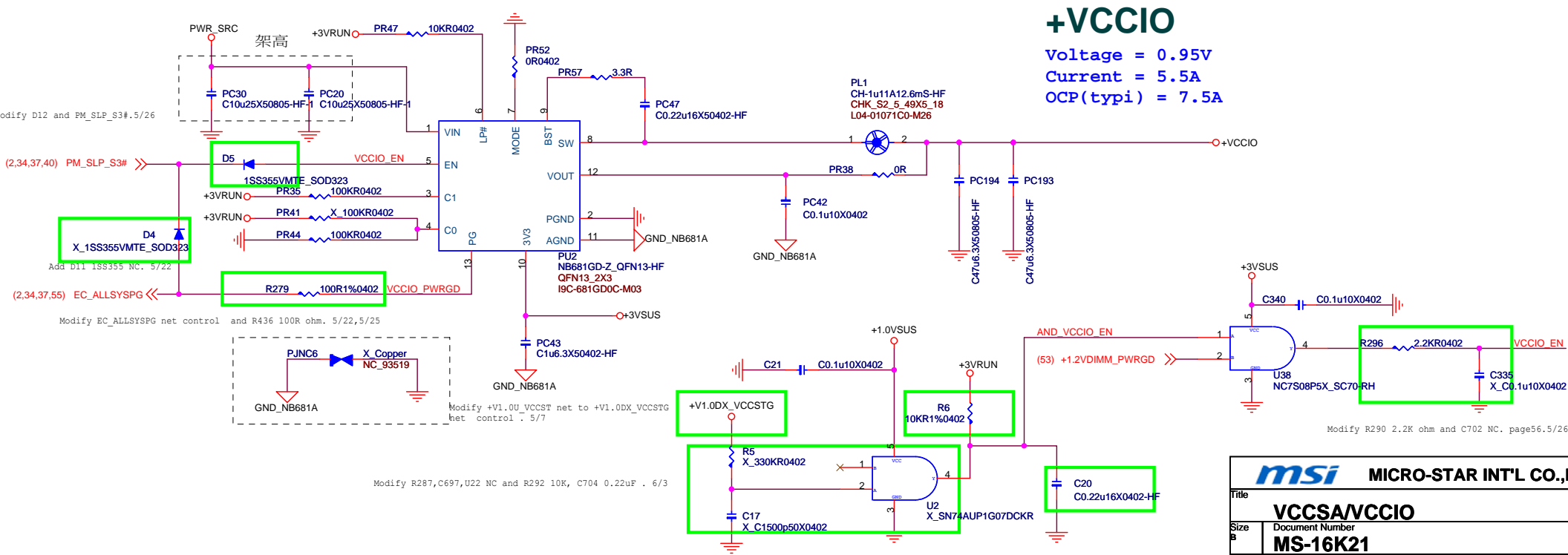
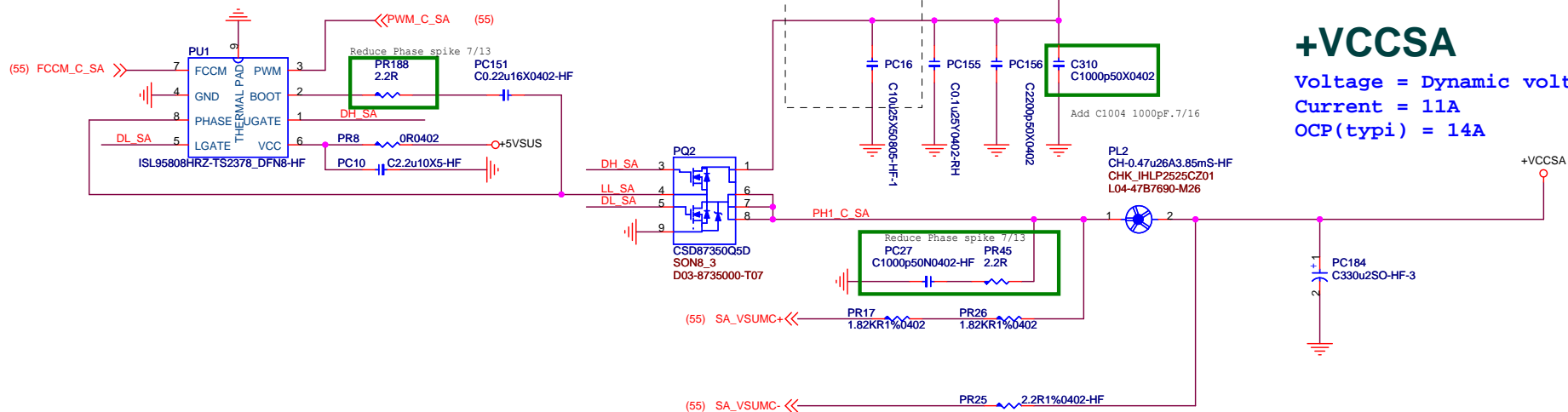
PROG1	110KR	Vboot=0V, Selw rate=30mV/us, VR_A=IA, VR_B=GT, VR_C=SA
PROG2	71.5KR	IMAX VR_A=70A, VR_A PSIL=1PH
PROG3	20.5KR	IMAX VR_B=60A, DROOP VR_B Active
PROG4	182KR	DROOP VR_A Active, DROOP VR_C Active, VR_A VR_B Frequency=750kHz
PROG5	78.7KR	IMAX VR_C=12A, Frequency=583kHz

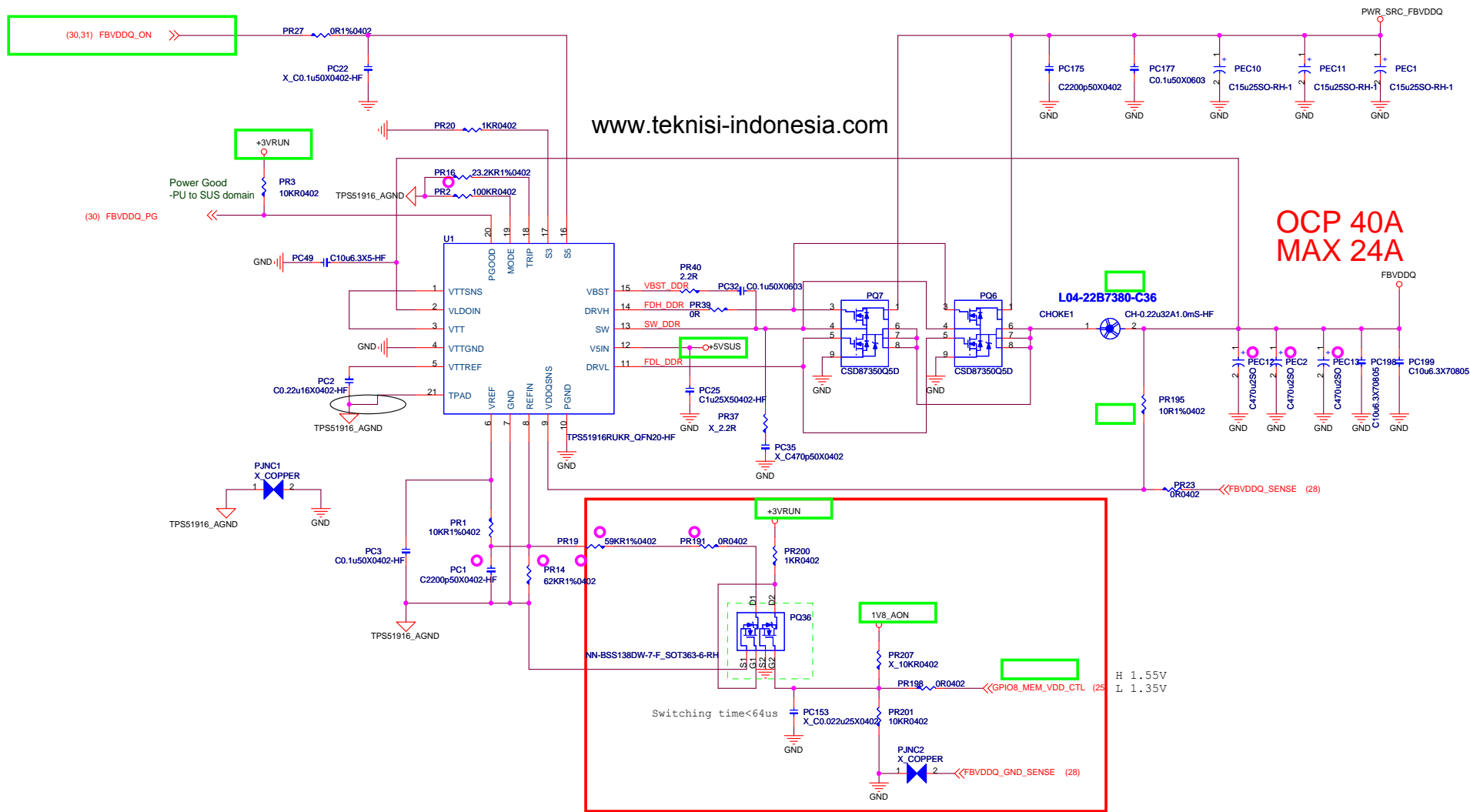
Follow Intel VIT Tools test to adjust 5/13





+VCCGT
Voltage = Dynamic voltage
Current = Iccmax 55A(<10ms)
OCP(typi) = 66A





DGPU POWER / UP9509P

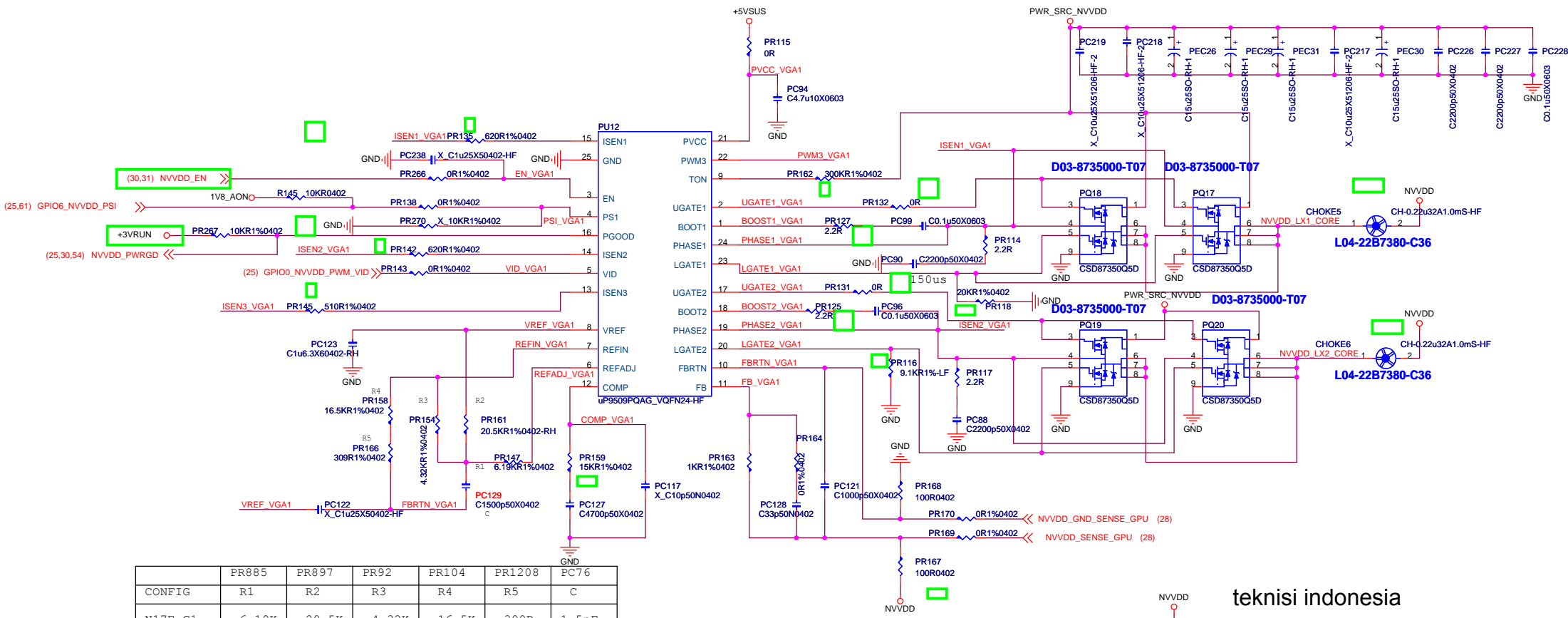
EDP-Peak 136A

EDP-Con 58A

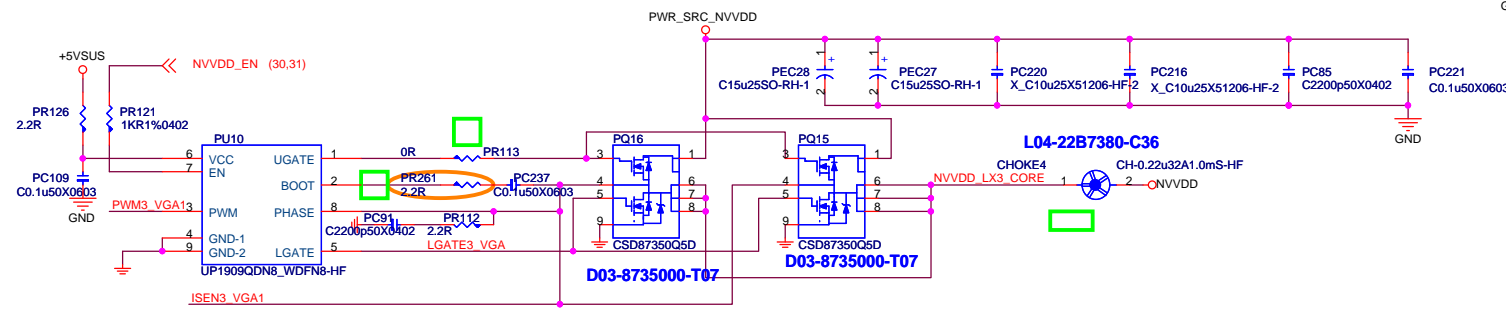
DGPU POWER NVVDD

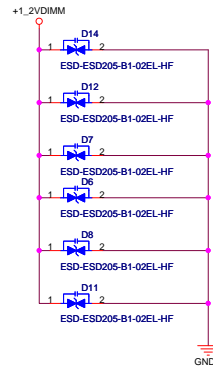
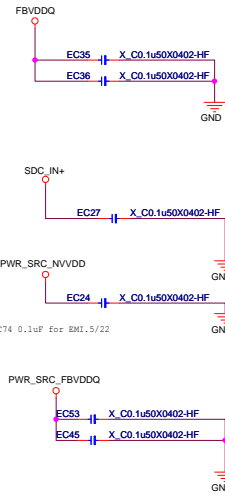
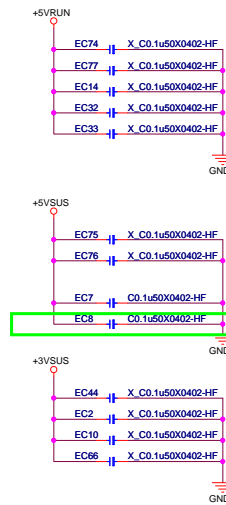
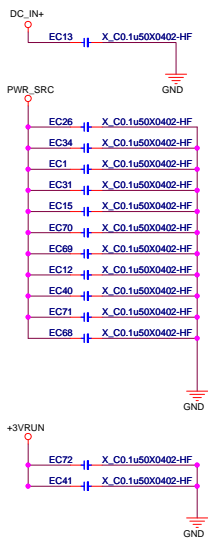
VBoot:0.8V

Vmin:0.3V / Vmax:1.3V

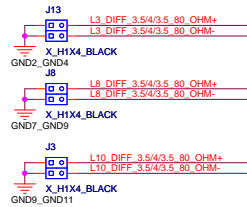


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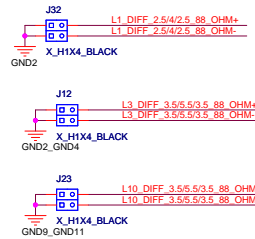




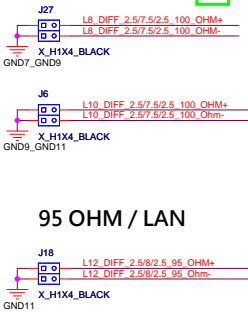
80 OHM / CLK/WCK



88 OHM / DDR4 CLK/DQS



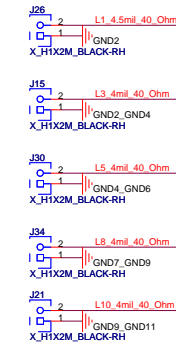
100 OHM / LAN



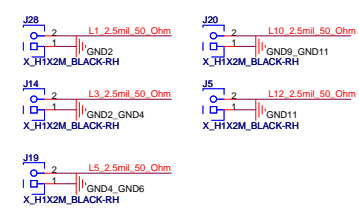
95 OHM / LAN



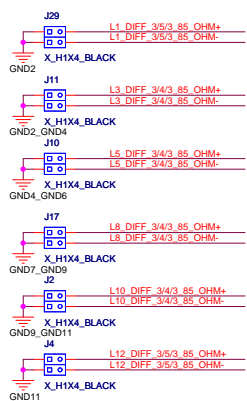
40 OHM / DDR4 CTRL



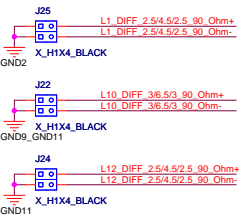
50 OHM / NORMAL / DDR4 DQ



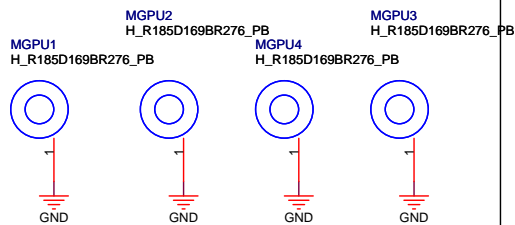
85 OHM / SATA /PCH PCIE/ EDP USB /HDMI/DP/DMI/CLK/PEG



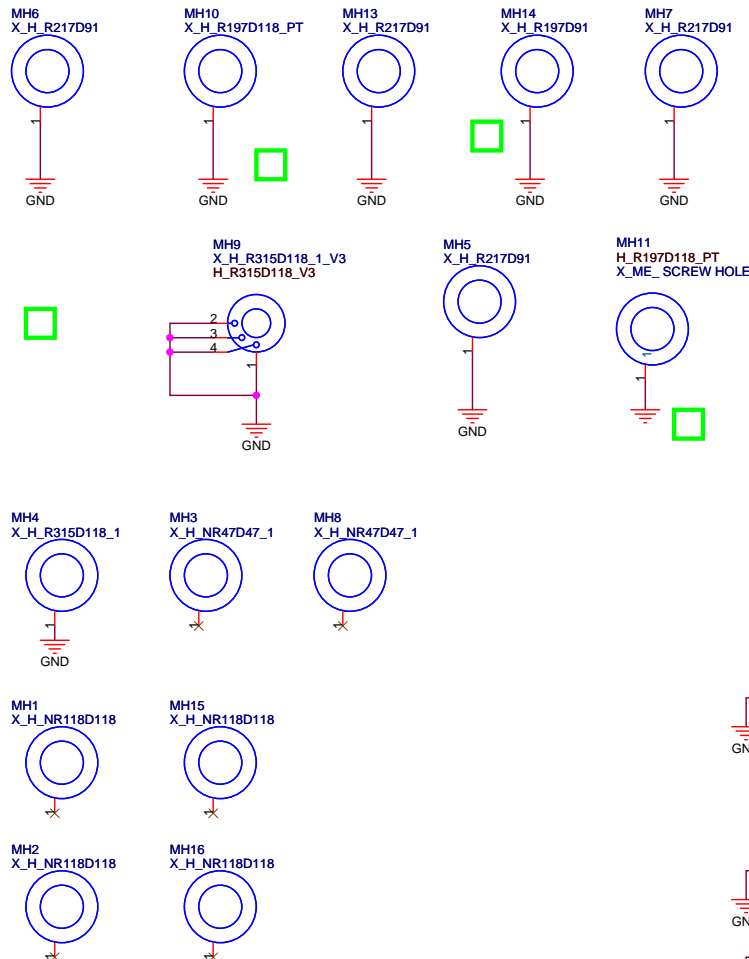
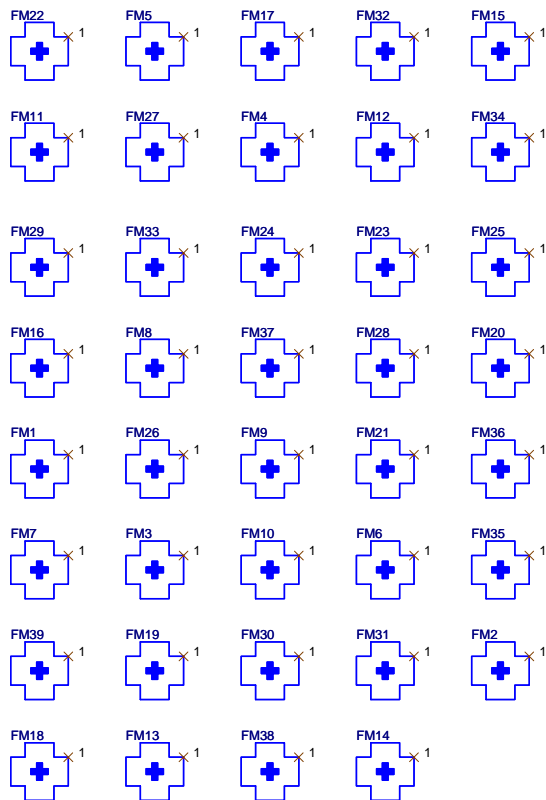
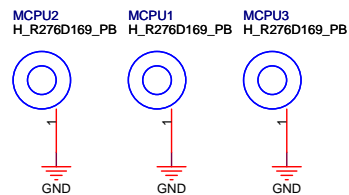
90 OHM / Alpine Ridge



dGPU Holes



CPU Holes



UME5
CPU BKT
CPU BRACKET
E2M-6K11211-HG0

UME4
MB
MYLAR
MB_mylar
E2P-6K11011-G40

UME7
GPU BKT
GPU_BRACKET
307-7B10111-Y77

PCB1
P30-16K210B-H73
P30-16K210B-H73

UME3
MB
MYLAR
X_MB_mylar
E2P-3F11111-Y42

RU1
E2Y-X006211-CA7
GASKET

RU2
E2M-3570611-G40
MECH

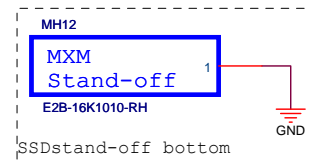
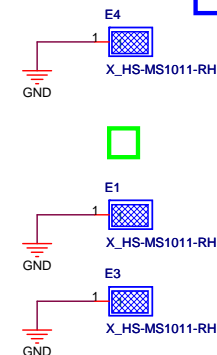
RU3
E2Y-3F10511-Y40
X_RUBBER

RU4
E2Y-3F10511-Y40
X_RUBBER

UME1
HDMI
Lable
X_HDMIROYALTY
Y01-RHDMI03-000

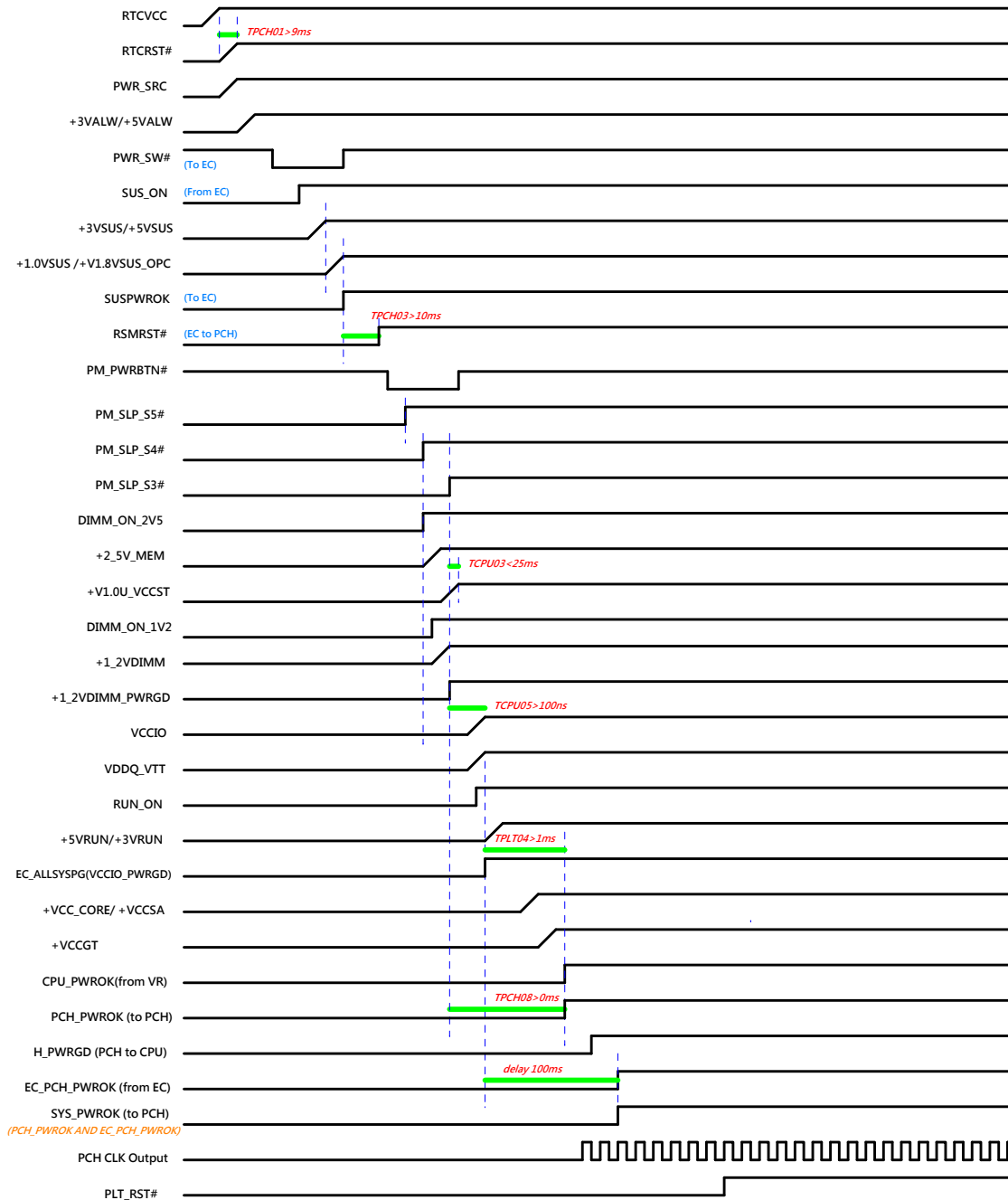
UME2
BIOS
Lable
X_UEFI_CODE_BIOS_LABEL
G51-N1CO041-A09

For MP



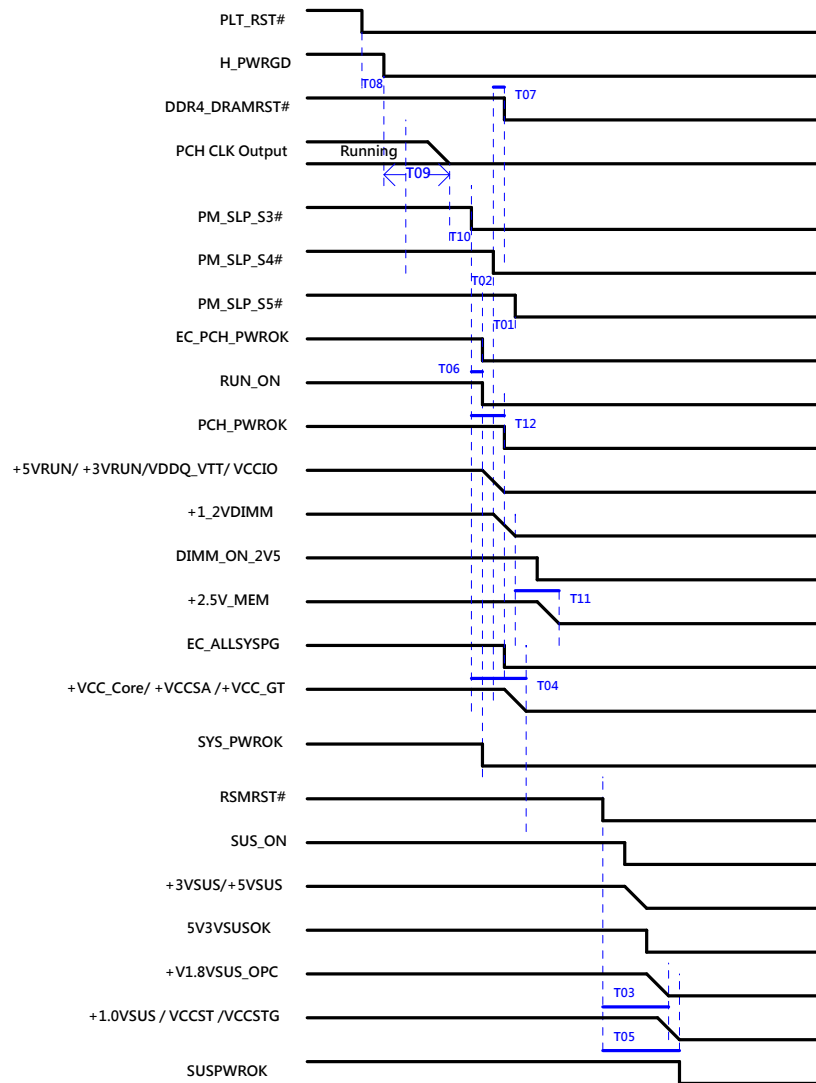
Power on Sequence

G3 -> S0



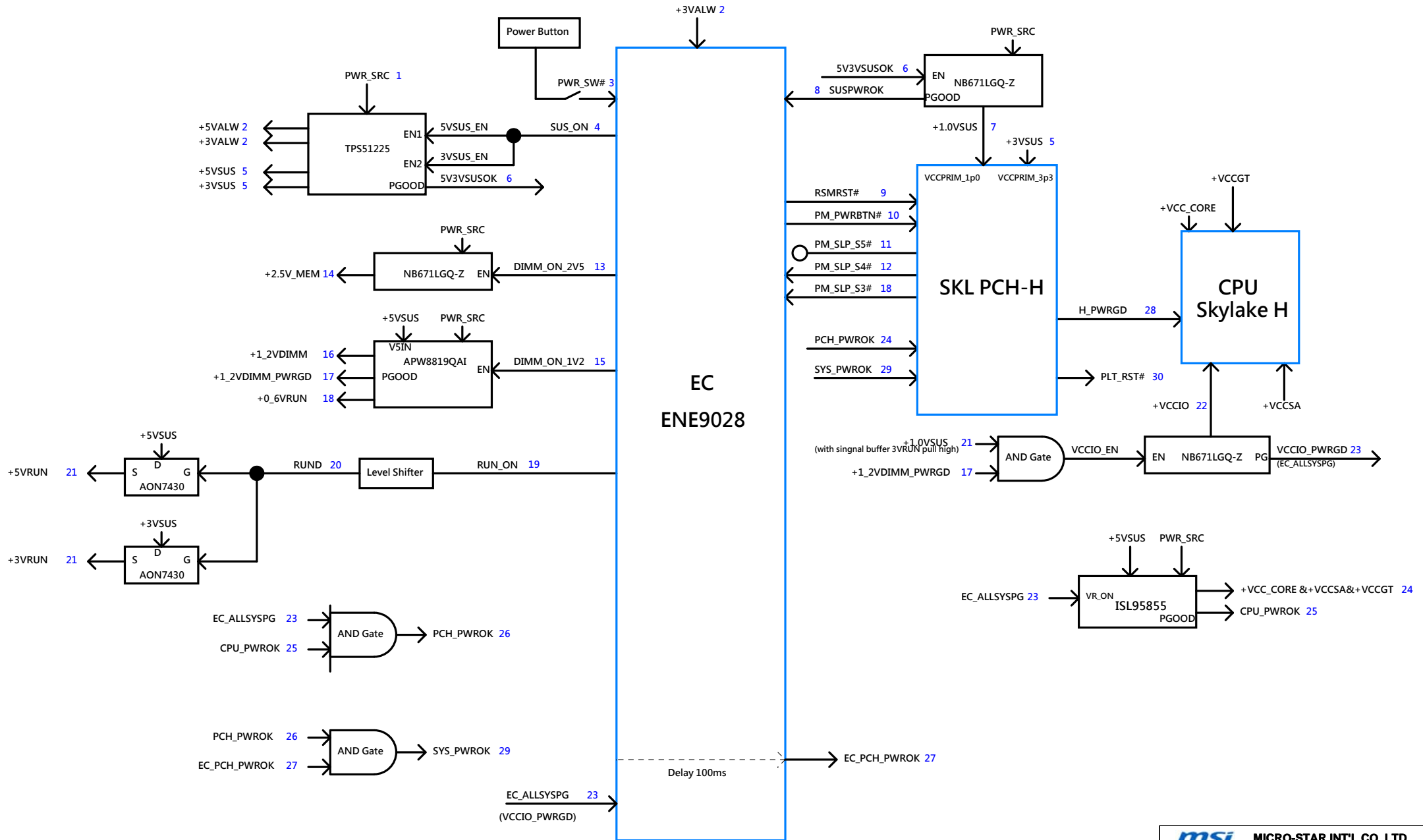
Power down Sequence

S0 -> G3



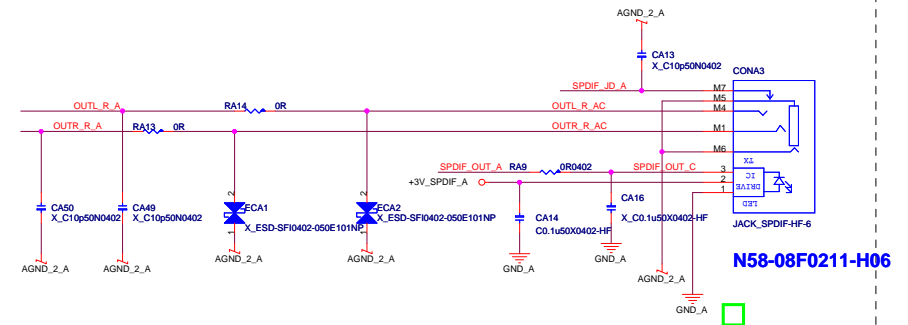
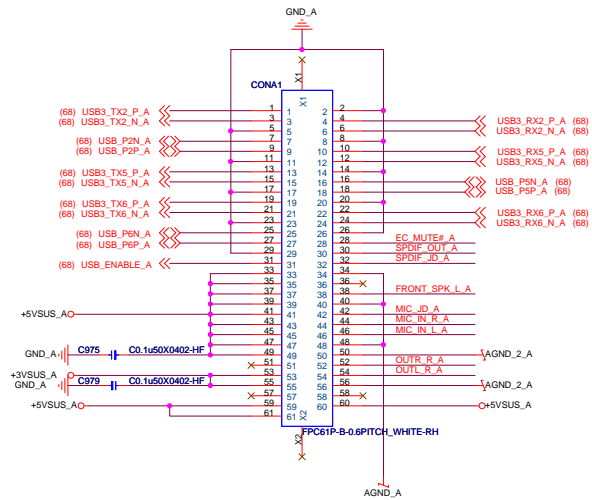
	MIN	MAX	Units	Description
T01	30		us	SLP_S5# assertion to SLP_S4#
T02	30		us	SLP_S4# assertion to SLP_S3#
T03	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T04		500	ms	SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.
T05	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T06		1	us	SLP_S3# assertion to VCCIO VR disabled
T07	-100		ns	DDR_RESET# assertion to SLP_S4# assertion
T08	30		us	PLTRST# assertion to PROCPWRGD deassertion
T09	10		us	PROCPWRGD de-assertion to CLKOUT_BCLK turning OFF.
T10	1		us	CLKOUT_BCLK turning OFF to SLP_S3# assertion
T11	30		ms	VDDQ ramped down to VPP ramp down
T12	0		ms	SLP_S3# assertion to PCH_PWROK deassertion

MS-16K2 Power on Block Diagram

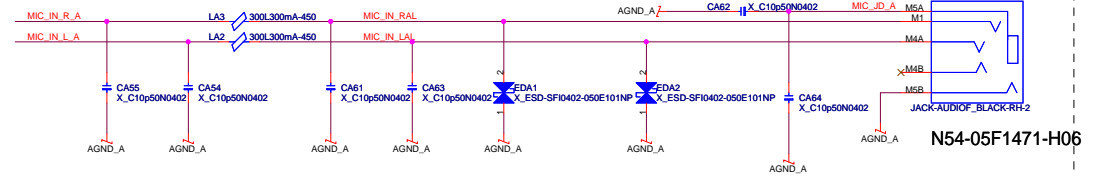


16K2-A Board (Audio CONN)

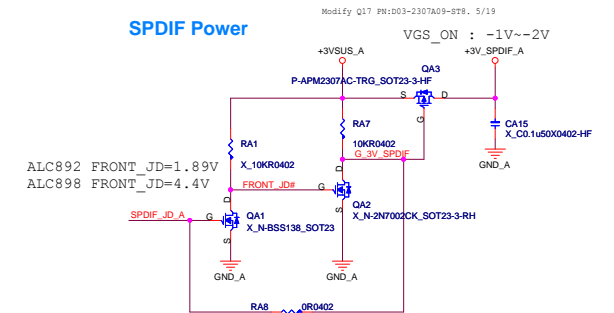
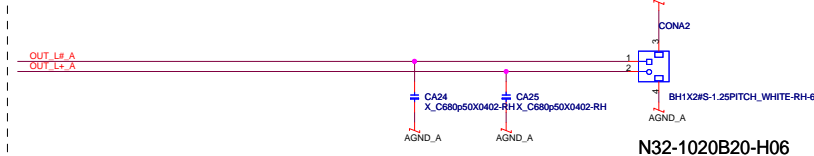
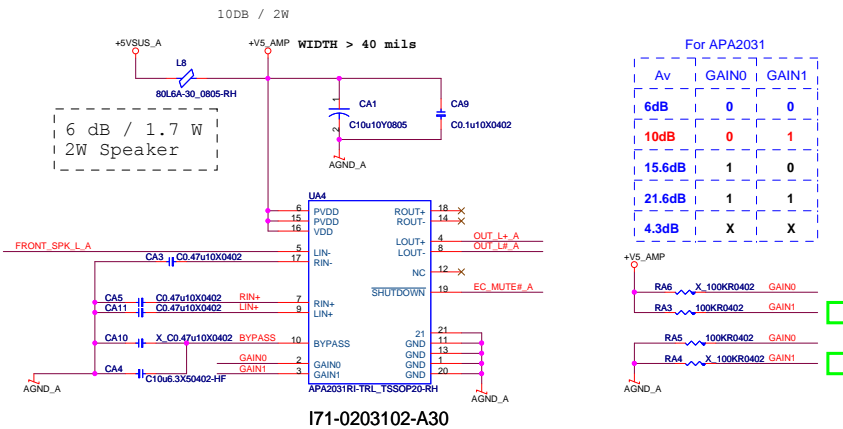
BTB Connector From MB
CONN Pin Current Capability : ???A/Pin



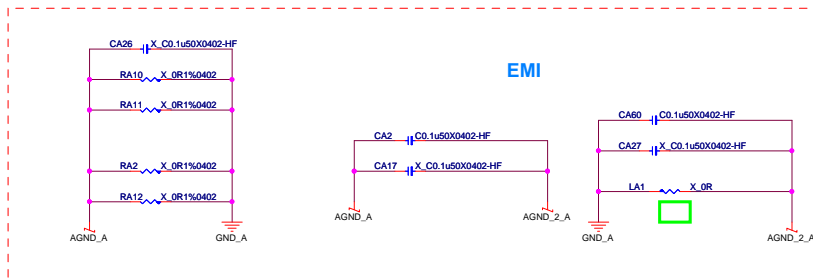
MIC IN

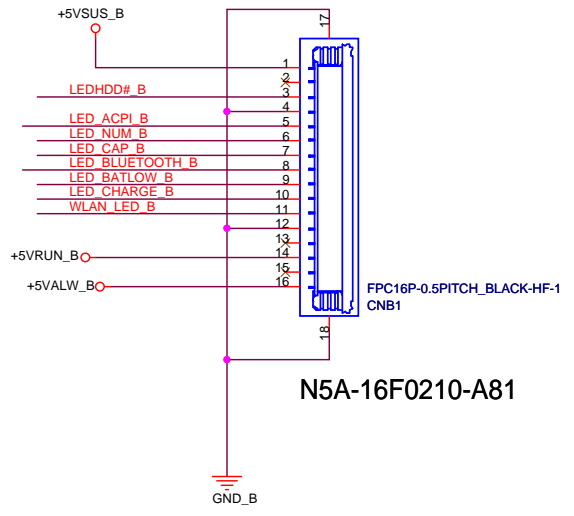
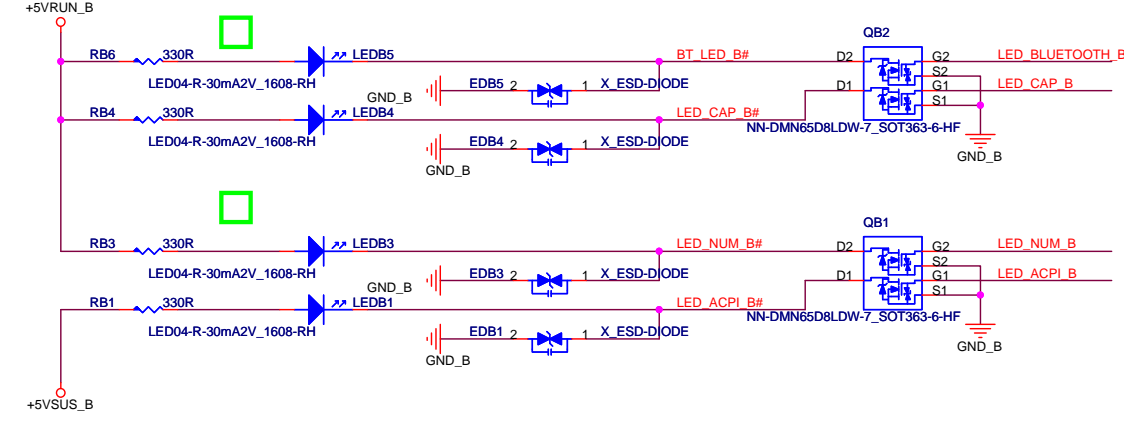
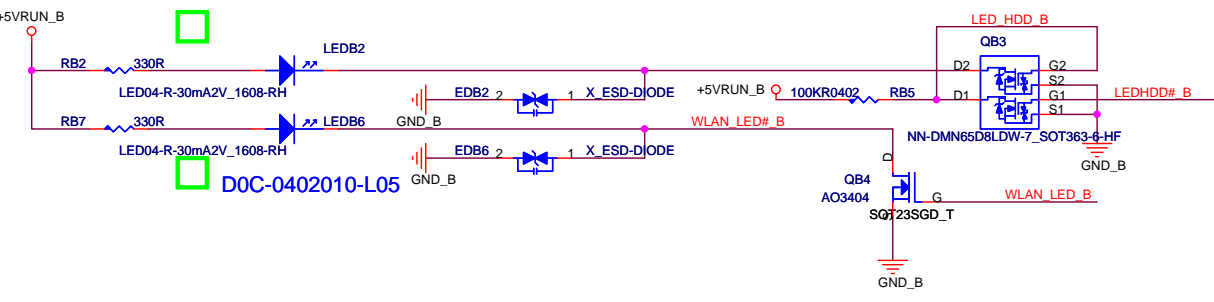
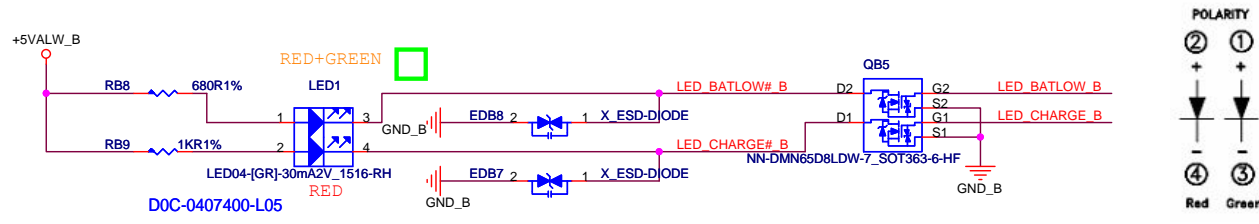


For 16K2

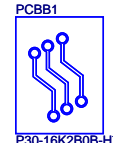


EMI

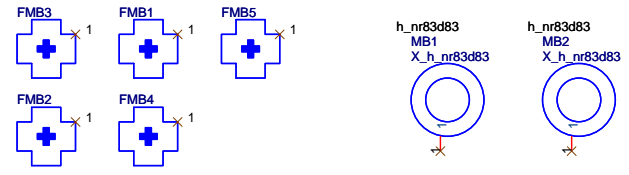




Hannstar: P30-14A1A0B-H73
TRIPOD: P30-14A1A0B-T53

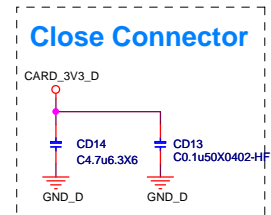
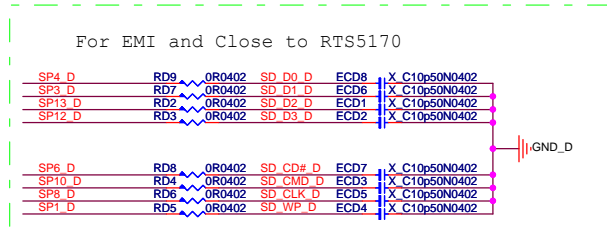
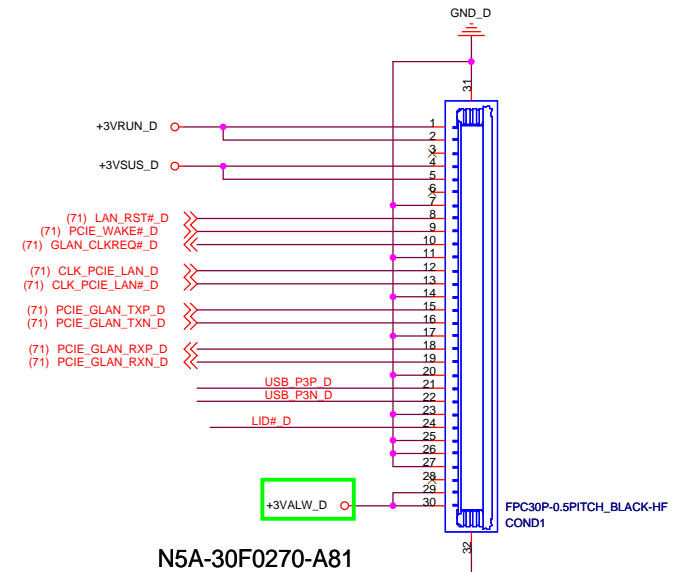
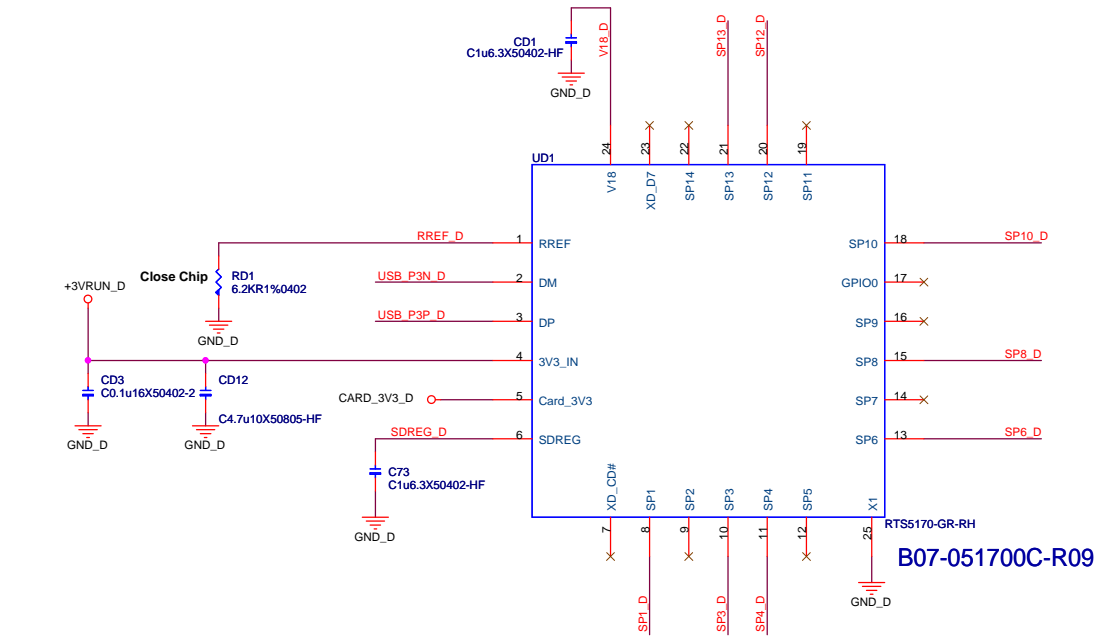


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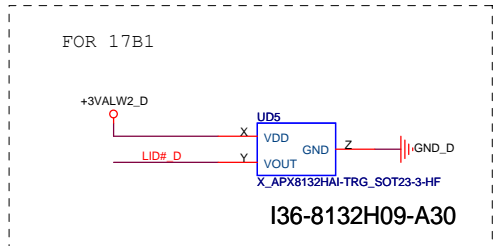
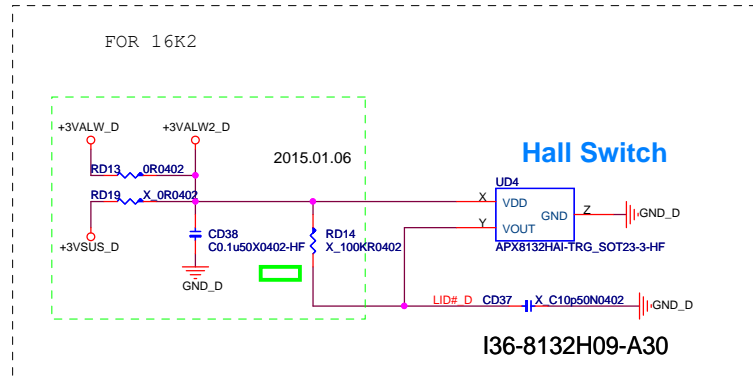
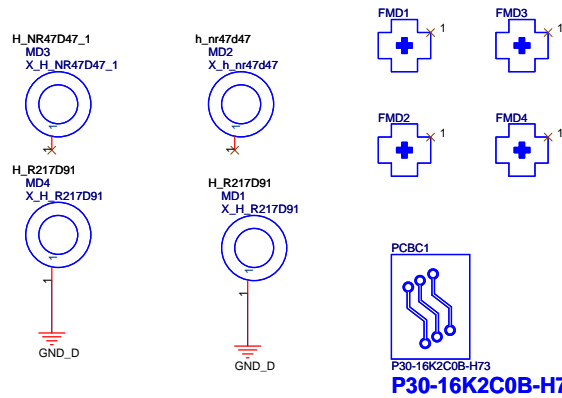
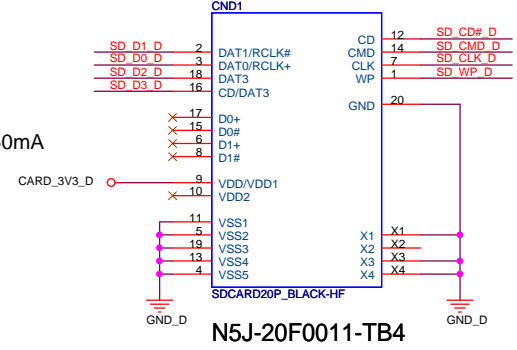


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Title	
[B] LED	
Size	Document Number
MS-16K2B	
Date:	Thursday, April 07, 2016
Sheet	69 of 73
Rev	0B

CardReader (RTS5170)

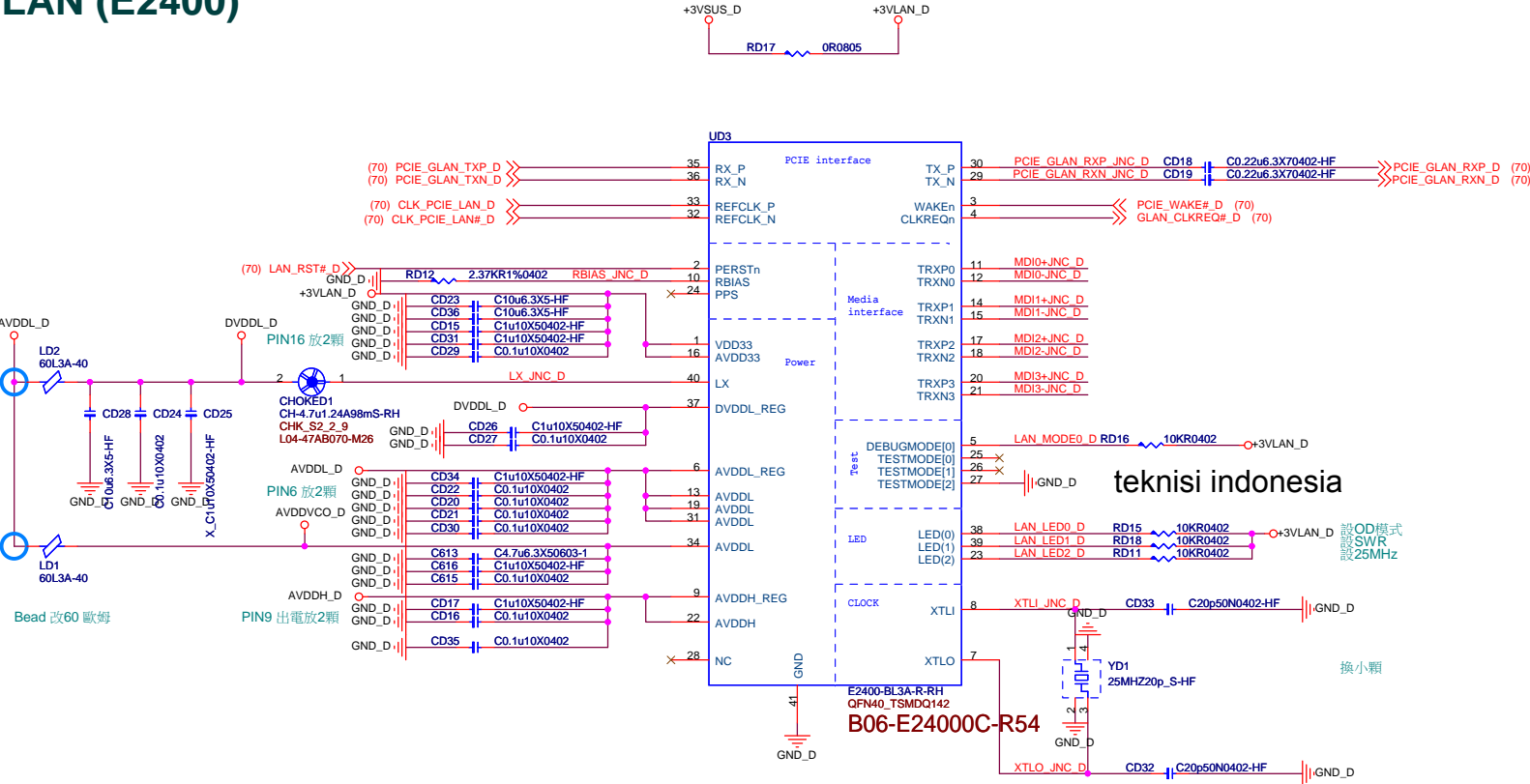


CARD_3V3: 950mA



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Title [C]Card Reader		
Size Custom	Document Number MS-16K2C	Rev 0B
Date: Wednesday, April 06, 2016	Sheet 70 of 73	

LAN (E2400)

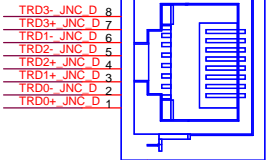
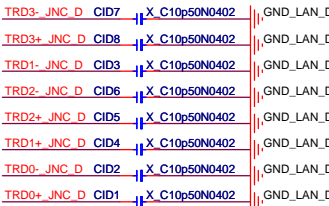


Use N-8600GS need RN4 EC18 NC and R866 on part.

MCT1 D RD10 X 10L500mA-200_0603-HF
Add colay AZ N-8600GS(OL5-7966001) R866 0ohm. 5/7
Modify R866 10L500mA for EMI.7/20

Modify C745,C710 10L300mA for EMI.7/20

EMI



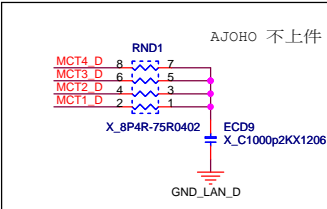
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Change CN6 PN. 7/13.

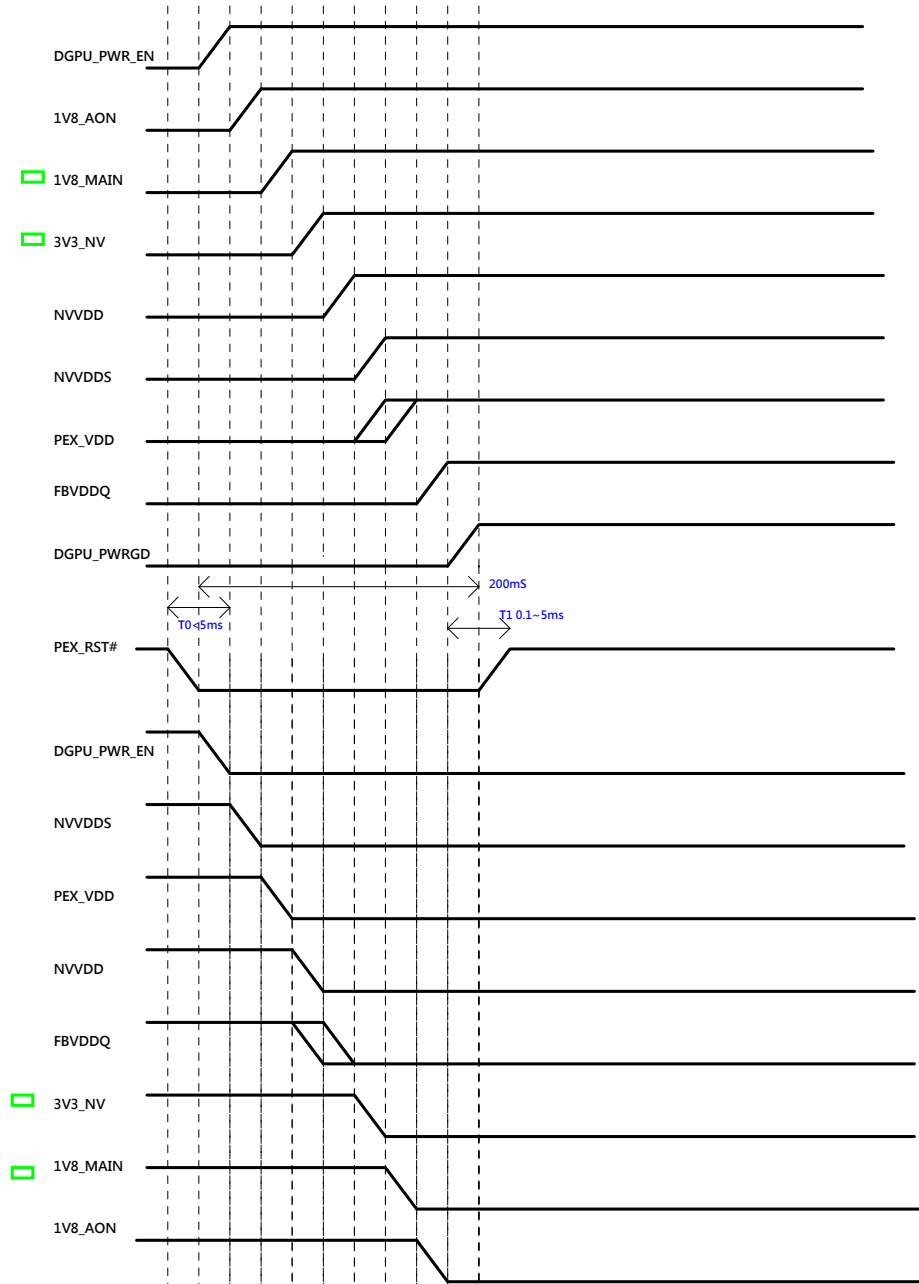
N55-08F0691-AF2

L05-0200300-A91

AJOHO 不上件




GPU Sequence



History

0B

DATE	PAGE	DESCRIPTION	DATE	PAGE	DESCRIPTION	DATE	PAGE	DESCRIPTION
0217	60, 61	1. REMOVE CHOKE3, PR124, PC98, PR122, PC230, PR257 NVVDDS 2相改1相 2. CHOKE1, CHOKE2, CHOKE4, CHOKE5, CHOKE6 CHANGE TO 10*10mm	0311	55, 56 57	1. Vcore PC182 → 680 pF (C11-6811812-W08) PC189 → NC PR215 → 95.3kohm (R11-9532T12-W08) PR46 → 3kohm (R11-0302T12-W08) Vgt PR182 → 84.5kohm (R11-8452T12-W08) PC15 → 470 pF (C11-4712012-T04) PC208 → NC PR199 → 3.16kohm (R11-3161T12-W08) Vsa PR43 → 88.7kohm (R11-8872T12-R01) PC172 → 1200 pF (C11-1222832-W08) NVVDDS PR258不上件 PR256上件	0311	60	1.PR116 改9.1K R11-0912T23-W08 (For ramp up time) 2.PR142, PR135 改 620ohm R11-0621T12-W08 3.PR162 改300K R11-0304T12-W08 4.PR159 改15K R11-0153T12-W08 5.PR118 改20K R11-0203T12-R01 6.PR145 改 510ohm R11-0511T12-W08 7.PR129 改24K R11-0243T12-W08
	63	1. REMOVE E2					69	1. CHANGE LED R TO 330R
0219	47	1. Change Y3 PN						
	54	1. PR92 CHANGE TO 3.92KOhm 2. PR84 CHANGE TO 300KOhm						
0301	30	1. ADD R549 1KOhm						
	30	1. CIRCUIT CHANGE TO PIN2						
0302	35	1. CHANGE U12 PN ,VCC CHANGE TO 1.8V	0314	39, 48	1. CHANGE EL9, EL10 FOOTPRINT			
0304	67	1. LA1 NO STUFF		43	1. CN11 PIN2&PIN3 SWAP 2. FPC2 PIN3&PIN4 SWAP			
0307	51	1. PR172 CHANGE TO 0.005Ohm						
	34	1. CN10 CHANGE +/- ,CHANGE BAT2 PN						
	59, 60 , 61	1. CHOKE1, 2, 4, 5, 6 CHANGE PN	0316	56, 57	1. PC187, PC190, PC192, PC200, PC201 改 C71-331037E-P01			
0309	69	1. CHANGE LED PN	0318	30	1. CHANGE 1V8MAIN & 3V3 SEQUENCE 2. ADD NVVDDS_PG DELAY CIRCUIT			
	32	1. R159 STUFF AND PU CHANGE TO PD		31	1. ADD 3V3_AON DISCHARGE CIRCUIT, ADD R559			
0311	37	1. ADD R241, Q40	0322	35	1. U30 CHANGE TO BIOS PN, REMOVE BIOS1			
	43	1. CHANGE PWR LED CIRCUIT ,REMOVE Q16	0325	30	1. ADD 1V8MAIN_EN DELAY CIRCUIT			
			0330	45 67	1. OUT_R 6dB->10dB 2. OUT_L 6dB->10dB ONLY FOR 16K2			

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Title

History

Size
A3

Document Number
MS-16K2

Rev
0B

Date: Wednesday, April 06, 2016

Sheet 73 of 73